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A Novel SPIC with a Simple APFC Circuit*

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Abstract: A novel SPIC(smart power IC) with a simple APFC(active power factor correction) circuit on one chip is proposed. The V_{bus}(bus voltage) with high power factor falls from 600V to 400V by using a delay circuit in which a long channel length NMOS is used to substitute a large biasing resistance to save chip area. The lower V_{bus} results in a smaller R_{on}(on-resistance) of power switcher, which reduces the power loss of the power devices, improves the efficiency of the circuit, and reduces the cost of circuits. An integrated high voltage over voltage protect circuit is also designed in the circuits. Theory and simulations both prove the correctness and availability of the design.

Key words: APFC; SPIC; duty cycle; bus voltage
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1 Introduction

SPIC (smart power IC), which merges the high-voltage power devices into CMOS logic and/or bipolar analog circuits on one chip, permits significant improvement and better stability in performance at a less loss[1]. But conflict between performance and cost restricts the SPIC to spread abroad. Chen[2] has invented a novel half-bridge power drive devices which can be integrated in SPIC and improves the performance of SPIC with lower cost. The SPIC used in electric ballast has very large market in the world, and many researches have been done in this aspect, such as IR[3], ST[4]. Since the power factor has become a very important parameter in ballast in order to improve the power factor at the same time, these companies have used specific APFC IC to correct the power factor. But the cost of the ballast is too high for the ballast to be widely used[3,5]. So IR has proposed a simplified APFC circuit for ballast with very low cost, the power factor (PF) could be over 0.95[3], which is shown in Fig. 1. However, the line bus voltage (V_{bus}) of the design is up to 600V. Because the R_{on} of switching device (MOSFET) is proportional in 2.5 power of the breakdown voltage[6]; this high voltage brings on lower efficiency of circuit. To improve the efficiency of the circuit, a novel method is proposed in this paper that keeps high power factor with a lower V_{bus} (the V_{bus} drops to about 400V). The R_{on} of the devices for 600V is about 2.3 times than that of 400V, so the V_{bus} drops to 400V, the R_{on} is the 1/2.3 of the 600V. That means the loss of the power devices decreases a lot with the same devices area and the efficiency of the circuit is higher. It is a good way that optimizing in circuit to make the design of power de-

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vices easier.

Moreover, a high voltage over voltage protection circuit is designed at the same time; this method makes SPIC working more safely.

2 Theory and circuit design

The diagram of the simple APFC circuit is shown in Fig. 1. The SPIC is designed to drive half-bridge power devices that provide the signal of

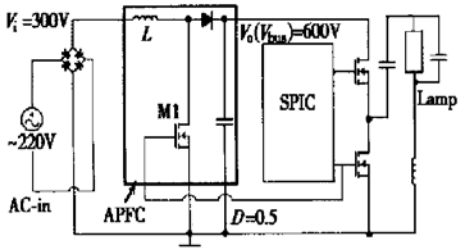

Fig. 1 Diagram of simply APFC circuit

40kHz to light the fluorescent lamp. The low side drive is a pulse with the duty cycle D of 0.5 that is commonly used in the APFC circuit. This circuit achieves to correct power. The expressions of the in-line voltage and the bus voltage in critical mode is shown as following[7]:

$$V_o = \frac{1}{1-D} V_i \qquad (1)$$

where V_i is in-line voltage and V_o is the bus voltage, the D is the duty cycle of the APFC switch. If D is 0.5, then V_o is $2V_i$, which means the rectified AC in-line voltage is DC 300V, and the V_o is 600V. So, if D reduces to 0.25, V_o(V_{bus}) is only about 400V. Since the D can not be too small, the Ref. [8] has pointed out that if the V_o/V_i is bigger than 1.25 (V_{bus} is higher than 375V), the PF can be kept higher than 0.95. So D = 0.25 is an acceptable choice. This pulse of D= 0.25 need not to be generated by outside control IC, and could be designed by a delay circuit. To save layout area, an improved circuit, which uses a very small current mirror[9] to charge the capacitance, is employed. This circuit has no large resistance and is shown in Fig. 2. The circuit includes pulse generating and pulse waveshaping circuits. The delay time is the time of charging capacitance. M2 and M4 are in the same V_{gs} named current mirror, which offer current to

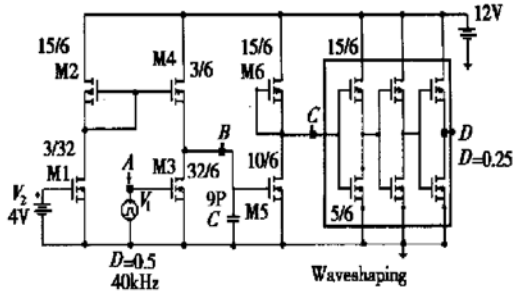

Fig. 2 Pulse generator circuit D= 0.25

M1 and M3, respectively. M3 is the active load of M4. M1 and the 4V voltage source replace the large biasing resistance. M6 is the active load of M5. The input pulse in point A is applied to M3. M3 works in two cases: (1) When the input is at high level, M3 turns on. Its gate width is 32μm. The discharge current is large enough to make voltage of point B drop to zero in very short time. The current of M4 flowes to GND at the same time. Point C is at high level. (2) When the point A changes to low level, the current of M4 charges the capacitance C, till the voltage of the point B rises to over the threshold voltage of M5(1V), M5 turns on, the point C changes to low level. So the charge time is delayed by capacitance C, and the charge time is delay time. In the case that the C is constant, the charge time can be decided by gate width of M4 and gate length of M1. The next three stage inverters are waveshaping circuits, which made the pulse good square wave. The output is at point D with D= 0.25 in this design. If the APFC circuit works in discontinuous-mode, the delay time is smaller and can be designed in this circuit by changing the channel length of M1 or the value of C.

The APFC circuit only changes the D, the other circuits need not be changed except a pin needs to be added to drive the APFC switcher, which the APDC drive signal can not be in common use with low side driving.

The high voltage over voltage protection is designed in the same chip according to the reference that reports a novel integrated high voltage detec-

tor[10]. The design is: the high voltage over-voltage protection mainly aims at the V_{bus}. The V_{bus} is decided by the BOOST raising voltage performance of the APFC circuit. The BOOST circuit is in the control of the switch M1 in Fig. 1. So if M1 turns off, the V_{bus} will never rise up. If the V_{bus} rises up over the protection value, a high voltage detector can detect this signal and transmit it to a comparator. The comparator outputs a signal to APFC driver circuit, which can turn off the M1. When M1 is turned off, the V_{bus} will keep at about 300V (DC) and never rises up to 600V (DC). The SPIC and power devices could be protected efficiently. The diagram of all the added circuits is shown in Fig. 3. The output signal of the pulse generator and the signal of the comparator are transmitted to an AND gate, then the AND gate outputs a signal to amplifier then to drive APFC switching M1. The protect bus voltage is chosen at 470V. The detail of the design refers to Ref. [10].

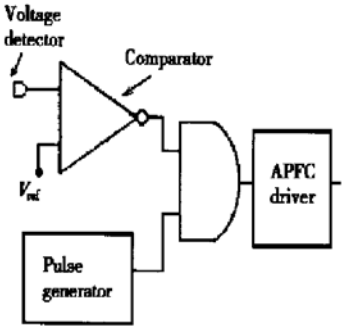

Fig. 3　Diagram of the added circuit

3　Simulation results and layout area estimate

The circuits were simulated using SPICE4. The devices' models are compatible with 2μm process. The circuit is shown in Fig. 2. For a 40kHz pulse with the duty cycle D = 0.5, the pulse with D = 0.25 is generated shown in Fig. 4. The results are shown in Fig. 4. The waveforms of key points named A, B, C and D. The waveform of point A is input pulse by the original circuit, point B is the charge voltage of capacitance, point C is the delayed pulse and point D is the shaped wave pulse with D = 0.25. The results prove the circuit to be effective.

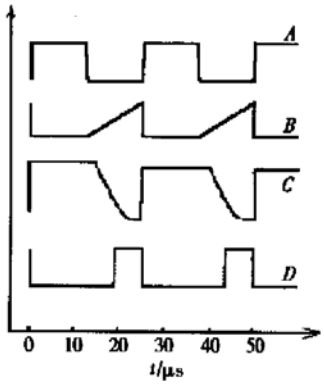

Fig. 4　Simple waveforms of simulation

The layout area is the cost of the SPIC. The added circuits with the drive circuit increase the area by about 12% of normal SPIC (without integrated power drive devices). On the other hand, the bus voltage drops to 400V. The layout of the voltage sustaining area of high-side tub and high-voltage shift circuits[3,4] would decrease by 4% at least. For the power devices integrated in SPIC[2], the saved area is about 8%. So the total added area is about 4%～8%, and this circuit would not increase the cost too much.

4　Conclusion

A novel SPIC with a simple APFC was proposed in this paper. The delay circuit, which employs a long channel length NMOS in place of large resistance to save layout area, can affords a pulse of duty cycle D = 0.25 to control the APFC switch, the bus voltage drop to 400V. The R_{on} of the power devices could be smaller with higher circuit effectivity; the power loss of the R_{on} decreases a lot. This is a good way to release the difficult in device design and save the cost of the power devices. Moreover, an integrated high voltage over voltage protect circuit is designed at the same time. All of the added circuits can be integrated in SPIC with-

out increasing the layout area too much. The circuit analysis and simulation proved that this design was applicable.

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一种新型的具有简易 APFC 的 SPIC 电路*

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摘要: 提出了一种新型的具有简易 APFC 的单片 SPIC 电路. 通过采用集成在 SPIC 内部的延迟电路, 使有 APFC 电路的总线电压由 600V 下降为 400V. 在电路中, 采用长沟道的 NMOS 管来代替大电阻以节省版图面积. 在保证所需的功率因数的情况下, 总线电压的下降可以直接导致功率开关器件的比导通电阻下降, 减小功率器件的损耗, 提高电路的效率. 同时, 总线电压下降, 也使电路成本降低. 此外, 还同时设计了相应的高压过压保护电路. 理论分析与模拟结果都证明该设计是正确的和有效的.

关键词: APFC; SPIC; 占空比; 总线电压

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