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Gate Current for MOSFETs with High *k* Dielectric Materials*

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Abstract: The MOSFET gate currents of high k gate dielectrics due to direct tunneling are investigated by using a new direct tunneling current model developed. The model includes both the inversion layer quantization effect with finite barrier height and the polysilicon depletion effect. The impacts of dielectric constant and conduction band offset as well as the band gap on the gate current are discussed. The results indicate that the gate dielectric materials with higher dielectric constant, larger conduction band offset and the larger band gap are necessary to reduce the gate current. The calculated results can be used as a guide to select the appropriate high k gate dielectric materials for MOSFETs.

Key words: MOSFET; direct tunneling; gate current; high k gate dielectric
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1 Introduction

With the scaling of MOSFETs into sub-100nm node, the thickness of gate oxide is projected to reduce to 1.5nm or below. Such an ultra-thin gate oxide will induce direct high tunneling gate leakage currents. Therefore, it is required for high dielectric constant (k) material to replace SiO_2 as gate dielectrics in order to reduce the high standby power[1]. The characteristics of sub-100nm MOSFETs with high k gate dielectrics, including the fringing-induced barrier lowering (FIBL) effect[2~5] and the properties of the stacked structure[6] have been studied. However, the effects of the material properties of high k gate dielectrics on the gate current have not been investigated carefully. But conventional gate current model can not describe the impact of band gap and band offset on the gate current.

Usually, the gate current passing through the MOS structure includes Fowler-Nordheim (FN) tunneling current and direct tunneling current. For thicker oxide and higher electric field, FN tunneling is dominant. Whereas, the direct tunneling becomes obvious for thinner oxide and lower electric field, thus direct tunneling is the main transport mechanism for the gate current flowing across the gate oxide layer between the gate electrode and the Si substrate, especially, for sub-100nm MOSFET operating range from 0.8V to 1.5V. For highly defective films, which have electron trap energy levels in the dielectric material band gap, current will be governed by the trap-assisted mechanism such as Frenkel-Poole emission J_{FP} or hopping conduction J_{hop}[12]. However, in this study, we focus on the impacts of dielectric material properties on the gate current. Only the gate dielectric thin films with lower defects density were considered. Thus only the direct tunneling currents were investigated without incorporating trap-assisted mechanism for sub-100nm MOSFET.

In this paper, we use a new direct tunneling current

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model developed by us to study the impacts of high k gate dielectric materials properties such as permittivity, band gap, and band offset on the MOSFET direct tunneling gate currents. The new direct tunneling current model includes the inversion layer quantization effect with finite barrier height[7] and the polysilicon depletion effect, where the modified WKB method[8] for calculating the transmission probability is adopted. The calculated results can be used as a guide to the selections of the dielectric materials for high k gate dielectric MOSFETs.

2 Gate current model

When MOSFET is scaled down to sub-100nm, the direct tunneling current will be dominant by the gate current of MOSFET. Here the direct tunneling current can be modeled by incorporating the inversion layer quantization effect with a finite potential barrier height as the boundary condition[7] and the modified WKB method[8,9] for calculating the transmission probability.

When nMOSFETs operate normally, the gate current mainly originates from the channel electrons tunneling through the gate dielectric. Due to the quantization effect, the transmission probability T has to be calculated for each subband. Thus within the effective mass approximation, transmission probability of the modified WKB approach[8,9] can be written as

$$T_{ij}(E_{ij}) = T_{R_{ij}}(E_{ij}) \times T_{WKB_{ij}}(E_{ij}) \qquad (1)$$

where E_{ij} is the electrons energy of the jth sub band in the ith valley that needs to be determined by the boundary conditions (φ_{OX}) corresponding to the finite barrier height as described in Ref. [7], $T_{WKB_{ij}}$ is corresponding to the transmission probability of the normal WKB approximation[11]. Based on the Franz-type dispersion relation $\frac{\hbar^2 \kappa_{ij}^2}{2m_{OX}} = \gamma_{ij} = E_{ij}\left(1 - \frac{E_{ij}}{E_{gOX}}\right)$, $T_{WKB_{ij}}$ can be written as

$$T_{WKB_{ij}} = \exp\left[\frac{E_{gOX}\sqrt{2m_{OX}}}{4\hbar eF_{OX_{ij}}}\left(2\gamma'_{ij}\sqrt{\gamma_{ij}} + \sqrt{E_{gOX}}\sin^{-1}\gamma'_{ij}\right)\right]\Bigg|_{E_{OX_{ij}} = e\varphi_{OX} - E_{ij}}^{E_{OX_{ij}} = e\varphi_{OX} - E_{ij} - eV_{OX}} \qquad (2)$$

where $F_{OX_{ij}} = (E_F - E_{ij})\frac{em_{3i}\varepsilon_k}{\pi\hbar^2}$ is the electric field and is obtained by using Gauss's law, m_{OX} is the effective mass for gate dielectric material, E_{gOX} is the band gap for the gate dielectric material, and $\varepsilon_k = k\varepsilon_O$. k is the dielectric constant of gate dielectric material, for instance, k value of SiO_2 is 3.9. $T_{R_{ij}}$ is a correction factor considering the reflections from all boundaries within the oxide[8,9], which is expressed as:

$$T_{R_{ij}} = \frac{4v_{Si}(E_{ij})v_{OX_{ij}}(\varphi_{cat})}{v_{Si}^2(E_{ij}) + v_{OX_{ij}}^2(\varphi_{cat})} \times \frac{4v_{Si}(E_{ij}+eV_{OX})v_{OX_{ij}}(\varphi_{an})}{v_{Si}^2(E_{ij}+eV_{OX}) + v_{OX_{ij}}^2(\varphi_{an})} \qquad (3)$$

where $v_{Si}(E_{ij}) = \sqrt{\frac{2E_{ij}}{m_{3i}}}$ and $v_{Si}(E_{ij}+eV_{OX})$ are the group velocities of the electrons incident and leaving the oxide, respectively. $v_{OX_{ij}}(\varphi_{cat})$ and $v_{OX_{ij}}(\varphi_{an})$ are the magnitudes of the purely imaginary "group velocity" of electrons at the cathode side and anode side respectively within the dielectric material and $v_{OX_{ij}} = \frac{1}{\gamma'_{ij}}\sqrt{\frac{2\gamma_{ij}}{m_{OX}}}$. The total direct tunneling can be obtained as[8,9]:

$$J = e\sum_{ij} N_{ij}T_{ij}/\tau_{ij} \qquad (4)$$

where $\tau_{ij} = \frac{j\pi\hbar}{E_{ij}}$, $N_{ij} = \left(\frac{kT}{\pi\hbar^2}\right)g_i m_{3i}\ln\left(1+\exp\left[\frac{E_F - E_{ij}}{kT}\right]\right)$ is the density of jth subband in the ith valley, g_i is the ith valley degeneracy, and m_{3i} is the electron effective mass for the ith valley. At the surface of (100) silicon, there is a 2 fold degenerate valleys with a large effective mass $0.916m_0$ and the 4 fold degenerate valleys with a light effective mass $0.190m_0$[7]. Then the direct tunneling current of the MOS structure can be calculated from Eqs. (1) ~ (4) as the function of applied gate voltage V_g, where

$$V_g = V_{FB} + V_{OX} + \varphi_s + V_{poly} \qquad (5)$$

V_{FB} is the flat-band voltage. V_{poly} is the voltage drop due to the polysilicon depletion, which can be written as:

$$V_{poly}=\frac{q\varepsilon_{Si}N_{gate}T_{OX}^2}{\varepsilon_k^2}\left(\sqrt{1+\frac{2\varepsilon_k^2(V_{gs}-V_{FB}-\varphi_s)}{e\varepsilon_{Si}N_{gate}T_{OX}^2}}-1\right) \tag{6}$$

where N_{gate} is the doping concentration of poly Si gate and T_{OX} is the physical thickness of gate dielectric.

The gate current model described above is a physical model for the electrons tunneling through the gate dielectrics without assumptions on the dielectric materials property. For different dielectric materials, the gate current can be obtained by just changing the material parameters such as permittivity, band gap, and band offset. Thus this model can be used as the guide to select the appropriate high k gate dielectric materials for MOSFETs.

In order to verify our direct tunneling model, the direct tunneling gate current vs gate voltage with different SiO_2 thickness was calculated and compared with the full quantum results (white symbols) and experiments results (gray symbols) of Lo *et al*.[10], as shown in Fig. 1. From the figure, it can be seen that the new direct tunneling model is in good agreement with the results of experiment and the full quantum numerical calculation.

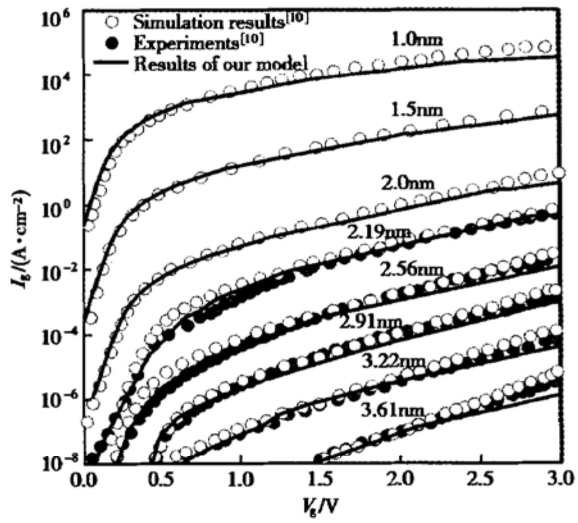

Fig. 1 Curves of direct tunneling gate current vs gate voltage with different thickness of SiO_2

3 Results and discussion

The influence of finite boundary condition on the direct tunneling currents of MOSFETs is compared for different gate dielectrics with different boundary conditions. The results are shown in Fig. 2, where bound-state corresponds to the infinite boundary condition and quasi-bound-state corresponds to the finite boundary condition. From the figure, it can be seen that the tunneling current under the finite boundary condition is larger than the one

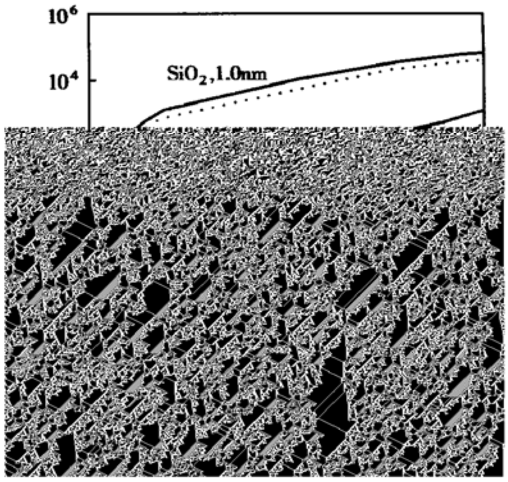

Fig. 2 Direct tunneling currents of MOSFETs with different gate dielectrics under different boundary conditions

under the infinite boundary condition. This can be understood since the wave function can penetrate into the gate dielectric under the finite boundary condition while the wave function becomes zero at the gate dielectric/Si interface under the infinite boundary condition. It also can be seen that, for the Si_3N_4 (φ_{OX} = 2.0eV) with equivalent oxide thickness EOT= 1.0nm, the difference of the direct tunneling current between the two boundary conditions becomes larger due to the lower barrier height. Usually the dielectric constant and band gap of a given material exhibit an inverse relationship, i. e. a higher dielectric constant material corresponds to a reduced band gap and lower bar-