Investigation of Gate Defects in Ultrathin MOS Structures Using DTRS Technique*

Huo Zongliang, Yang Guoyong, Xu MingZhen, Tan Changhua and Duan Xiaorong

(*Institute of Microelectronics, Peking University, Beijing 100871, China*)

Abstracts: A detailed description of relaxation spectroscopy technique under direct tunneling stress is given. A double peak phenomena by applied relaxation spectroscopy on ultra-thin (< 3nm) gate oxide is found. It suggests that two kinds of traps exist in the degradation of gate oxide. It is also observed that both the trap density and the generation/capture cross-section of oxide trap and interface trap are smaller in ultra-thin gate oxide (< 3nm) under DT stress than those in the thicker oxide (> 4nm) under FN stress, and the centroid of oxide trap is closer to anode interface than in the center of oxide.

Key words: tunneling; metal-oxide-semiconductor device; proportional difference operator

PACC: 7340G; 7340Q

CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2002)11-1146-08

1 Introduction

With the thickness of the gate oxide shrinking along device geometry, the reliability of gate oxide becomes an important issue. Especially for ultra-thin gate oxide with thickness less than 3nm, direct tunneling rather than Fowler-Nordheim tunneling of carriers through the gate oxide makes a significant contribution to the gate current[1~4]. This has big impact on power consumption and current drive for logic circuits and causes problems in data retention for memorycells. It is well known that high electrical field stresses lead to degradation of the device because trap charges can be generated at the Si-SiO_2 interface and inside the oxide during stress condition. However, no much is known about the failure induced by direct tunneling for ultra-thin gateoxide. Then, extracting and analyzing of defect information become special interest for understanding degradation induced by direct tunneling.

In order to separate and to determine oxide and interface traps, relaxation spectroscopy technique has been proposed and developed by Xu and Tan[5~10] for Fowler-Nordheim injection conditions for small dimension MOS device reliability analysis. Also, part of relaxation spectroscopy technique for direct tunneling injection conditions has been theoretically proposed[11]. However, detailed experimental information and further theoretical descriptions are needed.

In this article, direct tunneling relaxation spectroscopy is further described and applied in 1.9nm ultra-thin gate oxide. From our experiments, it is

* Project supported by National Science and Technology Program(No. G2000036503), University Doctoral Point Foundation

Huo Zongliang male, was born in 1975, PhD candidate. His research is degradation and breakdown mechanism of ultrathin gate oxide under uniform stresses.

Xu Mingzhen female, professor. She is interested in physics and characterization of small dimensional devices and reliability of semiconductor material and devices.

Tan Changhua male, professor. His research interests are in physics and reliability of small dimensional devices.

Received 14 May 2002

found that relaxation spectroscopy technique is still an effective, fast, and simple method to extract trap information for ultra-thin gate oxide with direct tunneling injection conditions. It is also observed that double peaks phenomena apparently exists, the trap density and the generation/capture cross-section of oxide trap and interface trap are smaller in ultra-thin gate oxide (< 3nm) under DT stress than those in the thicker oxide (> 4nm) under FN stress, and the centroid of oxide trap will be closer to anode interface than in the center of oxide.

2 Theory

2.1 Electron-fluence-dependence current equation for constant voltage stress

As the thickness of oxide decrease into ultra-thin stage, oxide voltage drops to a height below the oxide potential barrier height. That means that direct tunneling current must be considered rather than Fowler-Nordheim tunneling current. So, instead of classical FN formula, the tunneling current density under the condition of strong degenerate accumulation layer in the silicon substrate should be described as[2]

$$J_{DT} = \frac{A}{\left[1 - \left|\frac{\phi - qV_{ox}}{\phi}\right|^{1/2}\right]^2} E_{ox}^2 \times \exp\left[-\frac{B}{E_{ox}} \times \frac{\phi^{3/2} - (\phi - qV_{ox})^{3/2}}{\phi^{3/2}}\right] \quad (1)$$

where A and B are constants depending on the electron effective mass and barrier height ϕ at the cathode, V_{ox} represents the voltage drop over barrier layer, $E_{ox} = V_{ox}/T_{ox}$, and T_{ox} represents the oxide thickness. Equation(1) can be rewritten as

$$J_{DT} = \frac{A}{\alpha(E_{ox})} E_{ox}^2 \exp\left[-\frac{B}{E_{ox}} \beta(E_{ox})\right] \quad (2)$$

where $\phi = 3.15\text{eV}$

$$\alpha(E_{ox}) = \left[1 - \left|\frac{\phi - qT_{ox}E_{ox}}{\phi}\right|^{1/2}\right]^2 = [1 - (1 - \gamma E_{ox})^{1/2}]^2 \quad (3)$$

$$\beta(E_{ox}) = \frac{\phi^{3/2} - (\phi - qT_{ox}E_{ox})^{3/2}}{\phi^{3/2}} = 1 - 1(1 - \gamma E_{ox})^{3/2} \quad (4)$$

$$\gamma = qT_{ox}/\phi \quad (5)$$

As we know, high electric field stress generates trap charge inside the oxide. And the newly generated trap charge modifys oxide field. So, the field E_{ox} can be written as

$$E_{ox} = E_0(1 + \Delta E/E_0) \quad (6)$$

where E_0 represents the initial electric field corresponding to the initial tunneling current density J_{DT0}, and ΔE represents the change mount of electric field during the injection.

Usually, $\Delta E/E_0 < 1$, it can be verified from experiments. As shown in Fig. 1, the change of oxide field is not above 1% before oxide breakdown in

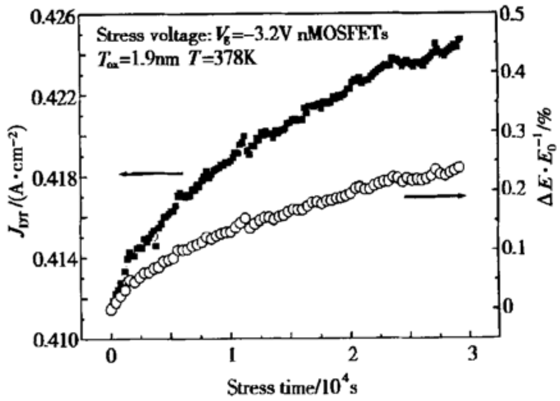

Fig. 1 Gate current density tunneling through ultra thin oxide dielectric of MOSFETs during constant voltage stress experiment and the corresponding electric field change

the experiments. So, Eq. (1) can be approximately rewritten as

$$\ln\left|\frac{J_{DT}}{J_{DT0}}\right| = H_{DT}\frac{\Delta E}{E_0} \quad (7)$$

where

$$H_{DT} = \left.\frac{d\{\ln[J_{DT}(E_{ox})]\}}{d(\Delta E/E_0)}\right|_{\frac{\Delta E}{E_0}=0} = 2 - \frac{\gamma E_0}{[1 - (1 - \gamma E_0)^{\frac{1}{2}}](1 - \gamma E_0)^{\frac{1}{2}}} + \frac{B}{E_0}\left[1 - \frac{3}{2}\gamma E_0(1 - \gamma E_0)^{\frac{1}{2}} - (1 - \gamma E_0)^{\frac{3}{2}}\right] \quad (8)$$

In our experiments, the value of parameter B and H_{DT} can be obtained as 283MV/cm and 5.69 respectively. Using the first-order rate equation and Gauss's law, the electric field change ΔE caused by the trapped and/or generated charges N_{ot} can be described by

$$\Delta E = -\frac{qX}{\epsilon_{ox}T_{ox}}N_{ot} = -\frac{qX}{\epsilon_{ox}T_{ox}}N_{ots}[1-\exp(-\langle\sigma_{ot}\rangle F)] \quad (9)$$

where ϵ_{ox} is the dielectric constant of the SiO_2, N_{ots}, $\langle\sigma_{ot}\rangle$, and X are the saturation density, the average generation/capture cross section of the oxide trap and the centriod measured from the anode, respectively. T_{ox} represents oxide thickness. $F = \int_0^t \frac{J}{q}dt$, is the electron fluence, where J represents the current density of direct tunneling. The effective oxide trap density $N_{ot,eff}$ can be obtained from Eqs. (7) and (9), as

$$\begin{aligned} N_{ot,eff}(F) &= \frac{X}{T_{ox}}N_{ot}(F) \\ &= \frac{X}{T_{ox}}N_{ots}[1-\exp(-\langle\sigma_{ot}\rangle F)] \\ &= N_{ots,eff}[1-\exp(-\langle\sigma_{ot}\rangle F)] \\ &= -\frac{\epsilon_{ox}E_0}{qH_{DT}}\ln\left|\frac{J_{DT}(F)}{J_{DT0}}\right| \end{aligned} \quad (10)$$

where $N_{ots,eff} = \frac{X}{T_{ox}}N_{ots}$, is the effective saturation density of oxide trap.

According to the method of proportional difference operator[5], the difference function of direct tunneling current can be written as

$$\begin{aligned} \Delta_p\ln(\frac{J_{DT}(F)}{J_{DT0}}) &= \ln(\frac{J_{DT}(K_pF)}{J_{DT0}}) - \ln(\frac{J_{DT}(F)}{J_{DT0}}) \\ &= -\frac{qH_{DT}}{\epsilon_{ox}E_0}\times\frac{X}{T_{ox}}N_{ots}[\exp(-\langle\sigma_{ot}\rangle F) \\ &\quad -\exp(-\langle\sigma_{ot}\rangle K_pF)] \end{aligned} \quad (11)$$

For peak position of current spectroscopy $F = F_{op}$, according to the extreme condition.

$$\frac{\partial\Delta_p\ln(\frac{J_{DT}(F)}{J_{DT0}})}{\partial F} = 0 \quad (12)$$

then, the following equation can be obtained

$$\langle\sigma_{ot}\rangle = \frac{\ln(k_p)}{k_p-1}\times\frac{1}{F_{op}} \quad (13)$$

$$\frac{X}{T_{ox}}N_{ots} = -\frac{\epsilon_{ox}E_0}{qH_{DT}}\Delta_p\ln(\frac{J_{DT}(F_{op})}{J_{DT0}})[k_p^{\frac{k_p}{1-k_p}}(k_p-1)]^{-1} \quad (14)$$

where F_{op} and σ_{ot} represent the peak fluence and capture cross-section for oxide trap density, respectively. $K_p = 1+\xi$, ξ is a small positive number.

2.2 Electron-fluence-dependence subthreshold gate voltage and swing

In many applications, threshold voltage is treated as an important characteristics parameter for processing and circuit. Usually, it is obtained from transfer characteristic curve. Just as we know, both charges of oxide trap and interface trap play important roles on the determination of threshold voltage. The oxide trap induces the shift of transfer characteristics curve. The interface trap induces the distortion of transfer characteristics curve. So, separation of traps will be important to understand the different components that contribute to the shift of threshold voltage. Here, our aim can be realized by analyzing sub-threshold characteristics with relaxation spectroscopy technique.

The shift of sub-threshold gate voltage, ΔV_{gw}, can be consisted of oxide trap and interface trap. It can be written as[9]

$$\begin{aligned} \Delta V_{gw} &= V_{gw}(F) - V_{gw}(0) = \Delta V_{wit} + \Delta V_{wot} \\ &= -(\frac{T_{ox}-X}{T_{ox}}\Delta Q_{ot}(F) + \Delta Q_{it}(F))/C_{ox} \end{aligned} \quad (15)$$

where

$$\begin{aligned} \Delta V_{wit}(F) &= -\frac{\Delta Q_{it}(F)}{C_{ox}}, \\ \Delta V_{wot}(F) &= -\frac{T_{ox}-X}{T_{ox}}\Delta Q_{ot}(F)/C_{ox} \end{aligned} \quad (16)$$

ΔV_{wit}, ΔV_{wot} represent the subthreshold gate voltage shift due to the interface and oxide trap generations under direct tunneling injection conditions, respectively. C_{ox} represents oxide capacitance. To separate both traps, subthreshold swing, S, usually can be adopted to characteristics of interface trap[12].

$$S = \ln 10\frac{dV_{gw}}{d\ln I_d} = S_0\frac{1+(C_d+C_{it})/C_{ox}}{1+C_d/C_{ox}} \quad (17)$$

where S_0 represents the subthreshold swing without interface traps. C_d represents the capacitance of depletion layer, C_{it} represents the capacitance of interface traps, $C_{it}= qN_{it}$, N_{it} represents the density of interface trap.

Also by using the first-order rate equation, the shift of subthreshold swing caused by interface trap charges can be written as

$$\Delta S(F) = S(F) - S(0) = \frac{qS_0}{C_{ox} + C_d}N_{it}(F)$$

$$= \frac{qS_0}{C_{ox} + C_d}N_{its}[1 - \exp(-\langle\sigma_{it}\rangle F)] \quad (18)$$

With the uniform distribution approximation of N_{it}[13], we have

$$\Delta Q_{it}(F) = \frac{C_{ox} + C_d}{S_0}\left(\frac{E_g}{2q} - \psi_B + \varphi_S\right)\Delta S(F) \quad (19)$$

where E_g represents the energy of silicon bandgap, ψ_B represents the potential of bulk Fermi.

Combining Eqs. (15) ~ (19), the effective density of oxide can be written as

$$\frac{T_{ox} - X}{T_{ox}}N_{ot}(F) = \frac{T_{ox} - X}{T_{ox}}N_{ots}$$

$$(1 - \exp(-\langle\sigma_{ot}\rangle F)) = -\frac{C_{ox}}{q}\Delta V_{gw}(F)$$

$$-\frac{C_{ox} + C_d}{qS_0}\left(\frac{E_g}{2q} - \psi_B + \varphi_S\right)\Delta S(F) \quad (20)$$

Similarly to Eq. (11), according to the difference of sampling spectroscopy theorem[9], we can get the following equations:

$$\langle\sigma_{it}\rangle = \frac{\ln k_p}{k_p - 1}F_{ip}^{-1} \quad (21)$$

$$N_{its} = \frac{C_{ox} + C_d}{qS_0}\Delta_p S(F_{ip})\left[k_p^{\frac{k_p}{1-k_p}}(k_p - 1)\right]^{-1} \quad (22)$$

$$\langle\sigma_{ot}\rangle = \frac{\ln(k_p)}{k_p - 1} \times \frac{1}{F_m} \quad (23)$$

$$\frac{T_{ox} - X}{T_{ox}}N_{ots} = \left(-\frac{C_{ox}}{q}\Delta_p V_{gw}(F_m) - \frac{C_{ox} + C_d}{qS_0}\right.$$

$$\left.\times\left(\frac{E_g}{2q} - \psi_B + \varphi_S\right)\Delta_p S(F_m)\right)\left[k_p^{\frac{k_p}{1-k_p}}(k_p - 1)\right]^{-1} \quad (24)$$

where F_{ip} and F_m represent the peak fluence for interface and oxide traps, respectively. $\langle\sigma_{ot}\rangle$ and $\langle\sigma_{it}\rangle$ represent the average generate/capture cross-section of oxide and interface trap, respectively. And N_{its}, N_{ots} represent the saturate interface and oxide trap density, respectively.

2.3 Extracting of oxide trap information

By combining Eqs. (14) and (24), the saturate density and centroid of oxide trap can be obtained as

$$N_{ots} = [D_{ot}(F_m) + D_j(F_{op})]\left[k_p^{\frac{k_p}{1-k_p}}(k_p - 1)\right]^{-1} \quad (25)$$

$$X = T_{ox}/\left(1 + \frac{D_v(F_m)}{D_j(F_{op})}\right) \quad (26)$$

where $$D_j(F_{op}) = -\frac{\varepsilon_{ox}E_0}{qH_{DT}}\Delta_p\ln\left(\frac{J_{DT}(F_{op})}{J_{DT0}}\right) \quad (27)$$

$$D_{ot}(F_m) = -\frac{C_{ox}}{q}\Delta_p V_{gw}(F_m) - \frac{C_{ox} + C_d}{qS_0}$$

$$\times\left(\frac{E_g}{2q} - \psi_B + \varphi_S\right)\Delta_p S(F_m) = \Delta_p V_{ot}(F_m) \quad (28)$$

3 Experiments and results

3.1 Sample

Experiments are performed by using HP4156B semiconductor parameter analyzer. The samples are n-channel MOSFETs with 10μm for both of channel width and channel length. The substrate is p-type Si with a resistivity of 0.1(Ω·cm) approximately. The thickness of gate oxide is approximately 1.9nm. Stress voltage (V_g) is −3.2V, while drain source and substrate are grounded. Flat-band voltage is approximately −0.95V. Experimental temperature is 105℃, controlled by temperature-controller. The direct tunneling stressing is interrupted after preset time intervals and transfer characteristics are measured at a drain voltage of 0.1V with source and substrate grounded. The sweep range of gate voltage is just enough to reveal the subthreshold characteristics, but not large enough to disturb the charge state of the gate oxide.

3.2 Experiments and results

From Fig. 1, it can be seen that stress current increases with stress time. It means that oxide trap charge changes oxide field as analyzing in 2.1. That means interface trap and oxide trap are generated during stressing. In order to extract and to separate oxide trap from interface trap, the shift of subthreshold gate voltage and the shift of subthreshold swing have been obtained from transfer characteristics shown in Fig. 2.

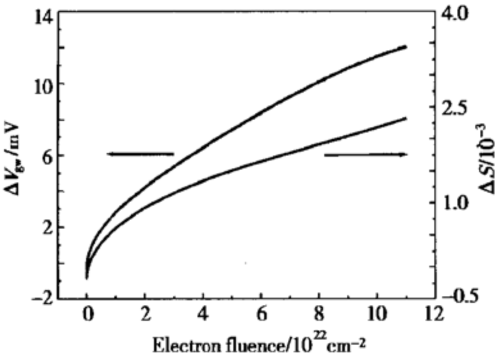

Fig. 2 Shift curves extracting from transfer characteristics

In order to extract oxide trap parameter, according to 2.1, proportional difference operator (PDO) curve of the shift of gate tunneling current, $\Delta_P\ln(J_{DT}(F)/J_{DT0})$, has been obtained from stress characteristics as shown in Fig. 3(a). From Fig. 3 (a), we can see that the proportional difference curve has obvious step, which means double peaks exist, and the phenomena of multi-trap interference[14] occurs. We think that double peaks mean two traps, and the change of gate tunneling current should be caused by the sum of two parts.

In order to verify our ideas, iterative method is adopted in separating PDO curve for single trap. As shown in Fig. 3(b), it is found that total PDO curve, $\Delta_P\ln(J_{DT}(F)/J_{DT0})$, which comes from proportional difference of the gate current shift, can be the sum of two proportional curve, $\Delta_P\ln(J_{DT}(F)/J_{DT0})_1$ and $\Delta_P\ln(J_{DT}(F)/J_{DT0})_2$. Then, we have the following relationship:

$$\Delta_P\ln(J_{DT}(F)/J_{DT0}) = \Delta_P\ln(J_{DT}(F)/J_{DT0})_1 + \Delta_P\ln(J_{DT}(F)/J_{DT0})_2 \qquad (29)$$

This means that our idea is reasonable, which proves that two traps play a role on the gate current during stress. So, with the help of the relaxation spectroscopy technique, the effect of different traps on oxide degradation can be studied separately.

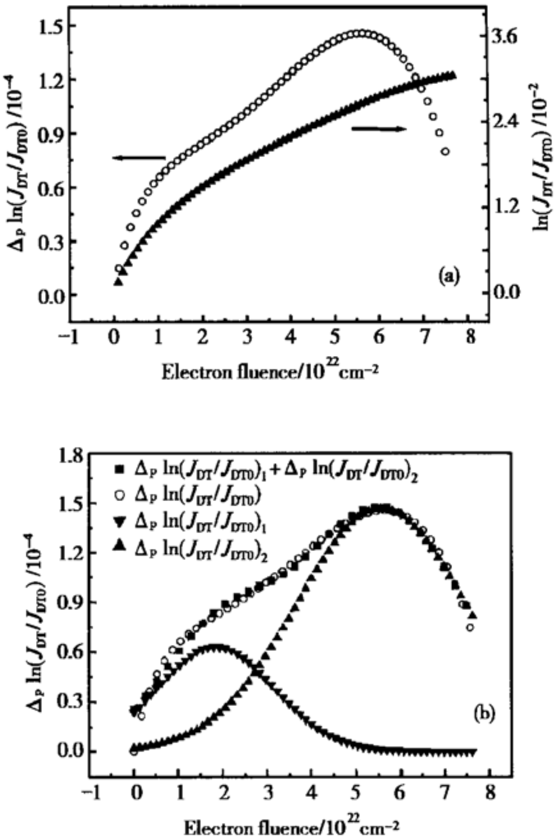

Fig. 3 (a) Typical proportional difference results for the shift of gate tunneling current; (b) Typical proportional difference for the shift of gate tunneling current Open symbols show experiment results; filled symbols show calculated results from iterative method

Similar to analysis in Fig. 3 (a) and (b), according to 2.2, the proportional difference operator curve of subthreshold gate voltage shift induced only by oxide trap and the proportional difference operator curve of subthreshod swing shift induced only by interface trap are also done as shown in Figs. 4~ 6. Here, Fig. 4 shows an example to explain the advantage of relaxation spectroscopy technique. By using the technique, double trap phenomena can be found easier in protional operator

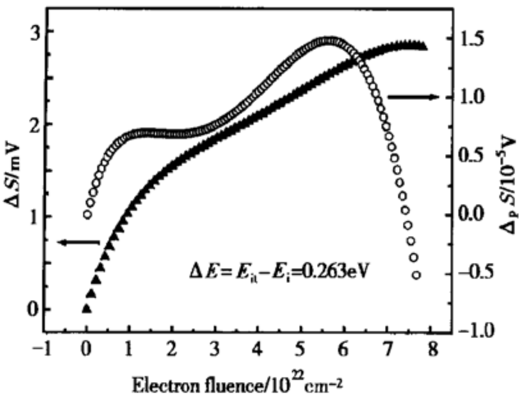

Fig. 4　Typical proportional difference for voltage shift induced by interface trap

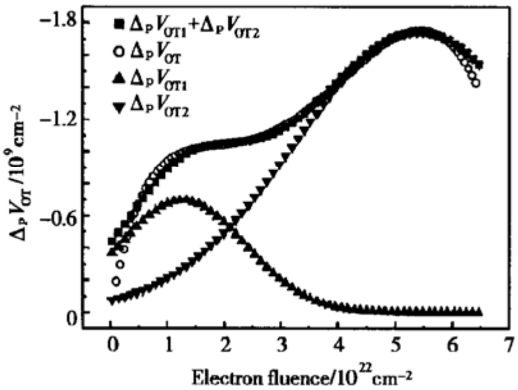

Fig. 5　Typical proportional difference for voltage shift induced by oxide trap　Open symbols show experiment results; filled symbols show calculated results from iterative method.

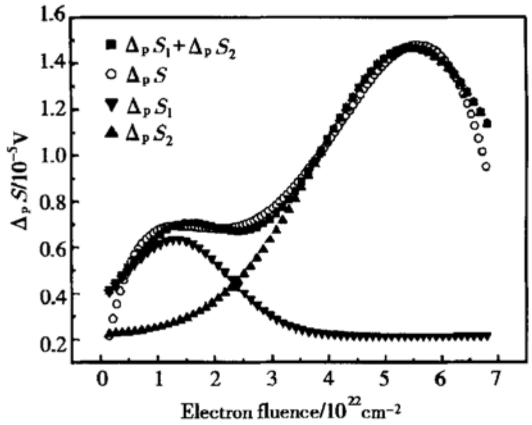

Fig. 6　Typical proportional difference for the shift of subthreshold swing　Open symbols show experiment results; filled symbols show calculated results from iterative method.

curve than in fresh curve. So, relaxation spectroscopy technique has high sensitive.

From Fig. 3, Fig. 5 and Fig. 6, we can see that double trap phenomena at the oxide interface and inside the oxide induced by direct tunneling stress current still exist in ultra-thin gate oxide similarly to thicker oxide in FN stress[9].

Based on our relaxation spectroscopy theory in 2.1~2.3, the following trap parameters can be obtained with an example of $k_p=1.01$:

$$\sigma_{it1}=8.98\times10^{-23}\text{cm}^2 \quad N_{its1}=2.64\times10^{11}\text{cm}^{-2}\text{eV}^{-1} \quad \text{at } E_{it}-E_i=0.263\text{eV}$$

$$\sigma_{it2}=1.78\times10^{-23}\text{cm}^2 \quad N_{its2}=6.12\times10^{11}\text{cm}^{-2}\text{eV}^{-1} \quad \text{at } E_{it}-E_i=0.263\text{eV}$$

$$\sigma_{ot1}=6.48\times10^{-23}\text{cm}^{-2} \quad N_{ots1}=-3.33\times10^{11}\text{cm}^{-2}$$

$$X_1=3.94\times10^{-8}\text{cm} \quad X_1/T_{ox}=0.21$$

$$\sigma_{ot2}=1.73\times10^{-23}\text{cm}^{-2} \quad N_{ots2}=-6.57\times10^{11}\text{cm}^{-2}$$

$$X_2=5.13\times10^{-8}\text{cm} \quad X_2/T_{ox}=0.27$$

It can be seen that both N_{ots} and N_{its} are smaller in ultra-thin gate oxide than those in thicker oxide (> 4nm), in which trap density for interface and oxide trap will be above 1×10^{12}cm^{-2}. Also it can be found that oxide trap located closer to Si/SiO_2 interface is different from that in thicker oxide, where centriod X approximately lies on the center of oxide, for example, $X\approx$2nm for 4nm gate oxide under FN stress. So, the phenomena of channel hot carrier noise becomes more obvious because of the fluctuation of channel carrier numbers induced by charge/discharge with near-interface oxide trap.

4 Conclusions

Detailed description of relaxation spectroscopy technique under direct tunneling stress has been demenstrated and applied in ultra-thin gate oxide. By combining proportional difference of gate current shift, sub-threshold swing shift, and subthreshold gate voltage shift, we got fast, simple and effective way to extract parameters of interface trap and oxide trap, such as the generation/capture cross-section, centroid, and density when a large direct tunneling current was injected through the gate oxide. Also by application in ultra-thin (1.9nm) gate oxide under DT stress, it is observed that double-trap behavior exists apparently. Experiments show that both the trap density and the generation/capture cross-section of oxide trap and interface trap are smaller in ultra-thin gate oxide (< 3nm) under DT stress than those in the thicker oxide (> 4nm) under FN stress, and the centroid of oxide trap is closer to anode interface than in the center of oxide.

Acknowledgements Thanks to Motorola Company for providing experimental samples and equipments. Thanks also to Dr. Wang Jinyan and Dr. Wang Ziou for helpful discussion.

References

[1] Momose H S, Ono M, Yoshitomi T, et al. 1.5nm direct-tunneling gate oxide Si MOSFET's. IEEE Trans Electron Devices, 1996, 43(8): 1233

[2] Depas M, Nigam T, Heyns M M. Definition of dielectric breakdown for ultra thin (< 2nm) gate oxides. Solid-State Electron, 1997, 41(5): 725

[3] Shih W K, Wang E X, Jallepalli S, et al. Modeling gate leakage current in nMOS structures due to tunneling through an ultra-thin oxide. Solid-State Electron, 1998, 42(6): 997

[4] Yang N, Henson W K, Hauser J R, et al. Modeling study of ultra-thin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices. IEEE Trans Electron Devices, 1999, 46(7): 1464

[5] Xu M, Tan C, Wang Y. Oxide current relaxation spectroscopy in tunneling metal-oxide-semiconductor structure under high field stresses. J Appl Phys, 1990, 67(11): 6924

[6] Xu M, Tan C, Wang Y. A new technique for determining the capture cross section of the oxide traps in MOS structures. IEEE Electron Devices Lett, 1991, 12(3): 122

[7] Tan C, Xu M, Wang Y. Application of the difference subthreshold swing analysis to study generation interface trap in MOS structures due to Fowler-Nordheim aging. IEEE Electron Device Lett, 1994, 15(7): 257

[8] Tan C, Xu M, Liu X, et al. Oxide trap relaxation spectroscopy: a new difference method to determine trap in oxidized silicon. J Appl Phys, 1995, 77(6): 2576

[9] Xu M, Tan C, He Y, et al. Dynamic oxide voltage relaxation spectroscopy. IEEE Trans Electron Devices, 1996, 43(4): 628

[10] Xu M, Tan C, He Y, et al. A spectral analysis method to directly determine minority carrier generation lifetime using the pulsed MOS structure. Solid-State Electron, 1994, 37(1): 31

[11] Wei Jianlin, Mao Lingfeng, Xu Mingzhen, et al. Direct tunneling relaxation spectroscopy in ultra-thin gate oxide MOS structures. Solid-State Electron, 2000, 44: 2021

[12] Sze S M. Physics of semiconductor devices. 2nd edition. John Wiley & Sone, 1981: 447

[13] Nicollian E H, Brews J R. MOS physics and technology. New York: Wiley, 1982: 492

[14] Xu M, Tan C, Liu X, et al. Effect of multi-trap interference on oxide current relaxation spectroscopy. ACTA Electronca Sinica, 1992, 20(5): 25

[15] Nigam T, Degraeve R, Groeseneken G, et al. A fast and simple methodology for lifetime prediction of ultra-thin oxides. IEEE Annual International Reliability Physics Symposium, 1999: 381

利用直接隧穿弛豫谱技术对超薄栅 MOS 结构中栅缺陷的研究*

霍宗亮　杨国勇　许铭真　谭长华　段小蓉

(北京大学微电子学研究所, 北京　100871)

摘要: 给出了超薄栅 MOS 结构中直接隧穿弛豫谱(DTRS)技术的细节描述, 同时在超薄栅氧化层(< 3nm)中给出了该技术的具体应用. 通过该技术, 超薄栅氧化层中明显的双峰现象被发现, 这意味着在栅氧化层退化过程中存在着两种陷阱. 更进一步的研究发现, 直接隧穿应力下超薄栅氧化层(< 3nm)中的界面/氧化层陷阱的密度以及俘获截面小于 FN 应力下厚氧化层(> 4nm)中界面/氧化层陷阱的密度和俘获截面, 同时发现超薄氧化层中氧化层陷阱的矩心更靠近阳极界面.

关键词: 隧穿; MOS 器件; 比例差分算符

PACC: 7340G; 7340Q

中图分类号: TN386　　**文献标识码**: A　　**文章编号**: **Article ID**: 0253-4177(2002)11-1146-08

* 国家科技攻关及高校博士点基金资助项目

霍宗亮　男, 1975 年出生, 博士研究生, 主要研究兴趣是 MOS 器件中超薄栅氧化层的退化和击穿机制.

许铭真　女, 教授, 主要从事小尺寸 MOS 器件特性及其表征、半导体材料可靠性物理和器件可靠性物理的研究.

谭长华　男, 教授, 主要从事小尺寸器件物理及可靠性物理的研究.

2002-05-14 收到