第 23 卷第 12 期　　半 导 体 学 报　　Vol. 23, No. 12
2002 年 12 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Dec., 2002

# Integrated Low-Power CMOS VCO and Its Divide-by-2 Dividers

Chi Baoyong and Shi Bingxue

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

**Abstract**: An integrated low-power CMOS VCO and its divide-by-2 dividers for WLAN transceivers are presented. The VCO is based on on-chip symmetrical spiral inductor and differential diode and the divide-by-2 dividers are based on the ILFD technique. Due to differential LC tanks and ILFD techniques, power consumption is low. The circuit is implemented in a 0.18μm CMOS process. Measurements show the proposed circuit could produce 3.6/1.8GHz dual band LO signals with a wide tuning range and low phase noise. 1.8GHz LO signals are quadrature. It consumes 5mA at $V_{DD}$= 1.5V. The size of die area is only 1.0mm×1.0mm.

**Key words**: VCO; WLAN transceivers; divide-by-2 divider
**EEACC**: 1230B; 7250E
**CLC number**: TN752　　**Document code**: A　　**Article ID**: 0253-4177(2002)12-1262-05

## 1 Introduction

Recently, integrated wireless local area network (WLAN) transceivers develop rapidly due to market demands. For the integrated wireless transceivers, a major challenge is the generation of local oscillator (LO) carrier signals[1~6]. Although a few literatures proposed GHz voltage-controlled oscillators (VCO), most of them are implemented in bipolar, GeSi, HBT, or GaAs process[7~10]. To implement full integrated wireless transceivers, it is necessary to take CMOS process to keep cost low and to be compatible with base band digital circuits. And many GHz transceivers incorporate quadrature-downconversion mixers due to their good image-rejection performance, it is difficult to generate exactly quadrature, low phase noise LO carrier signals. RC phase shift network, positive-/negative- edge triggered flip-flop, ring VCO and LC-VCO methods can be employed to generate quadrature LO signals but have many shortcomings due to large power consumption, low phase accuracy, bad gain matching and large phase noise[1~3,11].

The paper presents an integrated low-power CMOS VCO and its divide-by-2 dividers for WLAN transceivers. VCO is based on on-chip symmetrical spiral inductor and differential diode. And the divide-by-2 dividers are based on the ILFD technique. Due to differential LC tanks and ILFD techniques, the consumption of power is low. The circuit is implemented in a 0.18μm CMOS process. Measurements show the proposed circuit could produce 3.6/1.8GHz dual band LO signals with a wide tuning range and low phase noise. 1.8GHz LO signals are quadrature. It consumes 5mA at $V_{DD}$= 1.5V. The size of die area is only 1.0mm × 1.0mm.

Chi Baoyong male, PhD candidate. His work focuses on the analog circuit design and RF front-end circuit design.
Shi Bingxue male, professor and advisor of PhD candidates. His research interests include mixed-signal circuit design, VLSI implementations of artificial neural networks and fuzzy logic, DC-DC converters and RF circuits.

Received 13 June 2002, revised manuscript received 15 August 2002

## 2 Design details

Figure 1 shows the schematic diagram of the proposed circuit. There are three units: one VCO unit and two ILFD units. The output buffers are not included in the diagram.

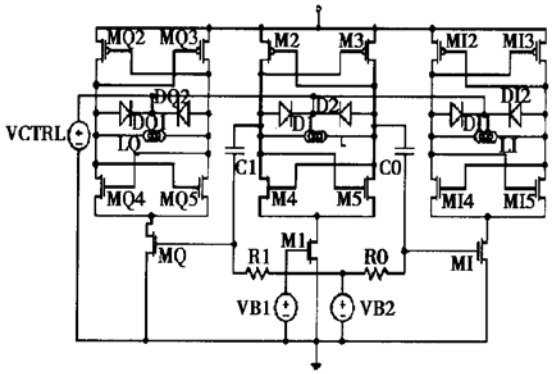


Fig. 1　Schematic diagram of the proposed circuit

VCO is a differential LC oscillator. Two pairs of cross-coupled transistors M2/M3 and M4/M5 generate the negative impedance required to cancel the losses of the LC tank, the M1 provides the tail current and is controlled by the bias voltage VB1. The LC tank is made up of an on-chip symmetrical spiral inductor and a pair of differential diode (shown in Fig. 2) to keep VCO full differential. Using differential LC tank improves its quality factor, has higher symmetry, and reduces LC tank die area almost by 50%. Since the inductor is the main source of loss in the LC tank and has a significant effect on the VCO power consumption and phase noise performance, it must be optimized to reach a high quality factor. A CAD analysis and simulation tool of inductors, ASITIC[5], was used to optimize the inductor and to extract the parasitic component parameters. The process provides 6 metal layers and 1 polysilicon layer. The winding of the inductor is made of the sixth metal layer while the transition section is made of the fifth metal layer. The optimized inductor is realized with an inductance 2.15nH, a shunt resistance 1100Ω and an area 200μm × 200μm. The inductor model is shown in Fig. 3 (a). The varactor is made up of a pair of differential diode modeled by Hspice Level 3 (or Spectre Level 1) diode model and a low resistor in series as showed in Fig. 3 (b). By careful layout design, the varactor has little effect on the quality factor of LC tank. In our design, each diode is laid out with 22 fingers, each 15μm wide, 0.5μm long and 0.5μm space.

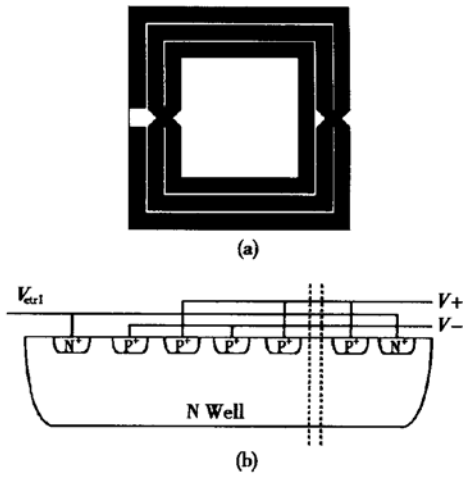


Fig. 2　(a) Symmetrical inductor; (b) Differential diode

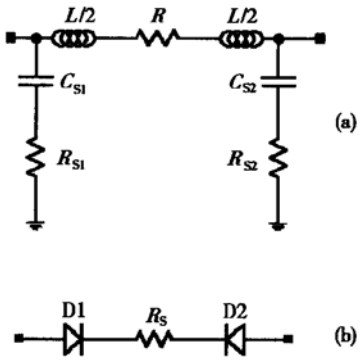


Fig. 3　(a) Spiral inductor SPICE model; (b) Differential diode SPICE model

The ILFD units are similar to the VCO unit. The VCO outputs are injected into the gates of ILFD tail current source MI and MQ as incident signals, and are delivered to common source connection nodes with a subunity voltage gain. The nonlinearity of MQ4/MQ5 and MI4/MI5 generates intermodulation products, which allow sustained oscillation at a fraction of the input frequency. As shown in Refs. [4, 6], in the special case of a di-

vide-by-2 divider and a third-order nonlinearity, the phase-limited locking range of an LC ILFD can be expressed as

$$\left|\frac{\Delta\omega}{\omega_f}\right| < \left|\frac{H_0 a_2 V_i}{2Q}\right|$$

where $\omega_f$ is free-running oscillation frequency, $\Delta\omega$ is frequency offset from $\omega_f$, $V_i$ is incident amplitude, $H_0$ is impedance of LC tank, $Q$ is quality factor of LC tank, $a_2$ is second-order coefficient of nonlinearity.

So one half of the incident signal frequency is only needed to keep inside the limited frequency offset range from free-running oscillation frequency, the ILFD will work well and the output will track the input frequency change. To reduce the circuit's dependence on nonliearity and to keep the circuit work well in all kinds of process variation, we use another strategy. The cross-coupled pairs and varactors in ILFD units are kept the same with VCO, and the inductance values of the inductors in ILFD are almost 4 times the one in VCO. So the free-running oscillation frequency of ILFD is approximately one half of the VCO output and there is no large frequency offset from free-running frequency, the ILFD units will keep locked without any risk.

The inductors in ILFD units are also symmetrical spiral inductor and made of the same layers with the one in VCO. After optimization by using ASITIC[5], the inductors are realized with an inductance 8.55nH, a shunt resistance 1248Ω and an area 240μm×240μm.

In the locked state, the ILFD unit is a divide-by-2 divider. By injecting the differential VCO outputs into two same ILFD units, we could get quadrature LO carrier signals with one half of the VCO frequency. The principle is similar to positive-/negative-edge triggered flip-flop method, the difference is only to use ILFD units as divide-by-2 dividers instead of flip-flops and the presented method will lower the power consumption. Since the ILFD units have a locked range and the VCO outputs are completely differential, mismatching of LC tanks and transistors in two ILFD units has little effect on the quadrature performance of the ILFD outputs. So the ILFD outputs are quadrature with almost no phase error, no gain mismatching and low phase noise. (Its phase noise is better than VCO due to the divide-by-2 dividers operation[4,6].)

The capacitors C0 and C1 remove the common mode components in the VCO outputs. The bias voltage VB2 is added to the gates of MI/MQ (as tail current source of ILFD units) through large resistors R0 and R1.

## 3 Measured results

To verify the performance, the proposed circuit was implemented in 0.18μm process. Figure 4 shows its microphotograph. The sized die area is only 1.0mm×1.0mm, and most of it was occupied by pads and three on-chip symmetrical spiral inductors.

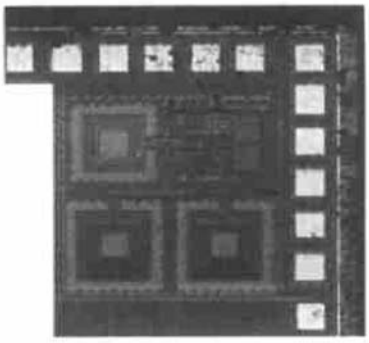

Fig. 4 Microphotograph of the proposed circuit

Hspice and Spectre RF simulations were done to judge the performance of the proposed circuit. Figure 5 shows the transient waveforms of differential outputs from two ILFD units; the VCO differential outputs are also showed in the same figure to show the tracking characteristic of ILFD units. From the figure, it could be seen that the ILFD units track incident signal very well as divide-by-2 dividers and their outputs are quadrature, with 90° phase difference and same amplitude. The quadrature performance is also verified with Spectre RF

PSS analysis. The results show that there are no phase error and gain mismatching in the EDA tool precision range. So the LO signals from the ILFD units are completely quadrature.

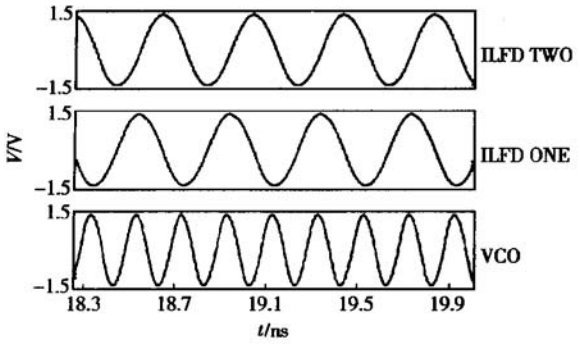


Fig. 5　Transient simulated waveforms

Figure 6 shows the measured tuning characteristics of the proposed circuit. The VCO tuning range is from 3.21GHz to 3.62GHz for a control voltage range of 0.5 ~ 2.0V at $V_{DD}$ = 1.5V. Due to divide-by-2 divider operation, the quadrature outputs from ILFD units have a tuning range of 1.60GHz to 1.81GHz, which is verified by Fig. 6(b). So the proposed circuits could generate 3.6/1.8GHz dual band LO signals. The tuning range is wide if we consider that we use the diode pairs as varactors instead of accumulated MOS. The power consumption is 5mA at $V_{DD}$ = 1.5V when six output buffers are included.

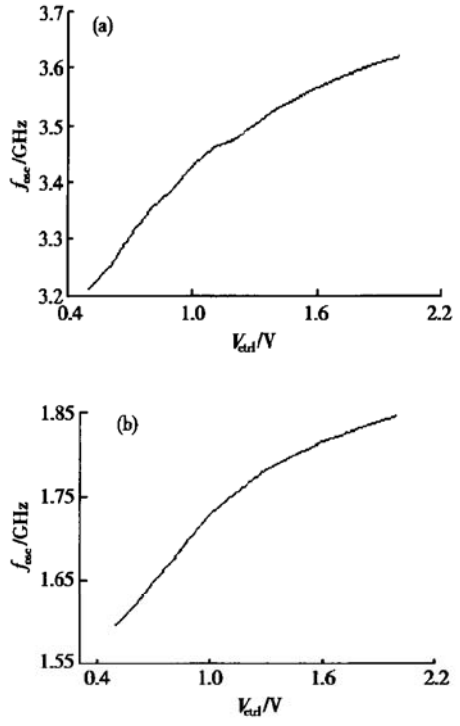


Fig. 6　Measured VCO oscillation frequency versus control voltage　(a) 3.6GHz VCO; (b) Divide-by-2 dividers

Figure 7 shows the phase noise for 3.54GHz VCO. The VCO has a phase noise -107.33dBc/Hz at 600kHz offset at 3.54GHz. As to the ILFD units, it has a phase noise 2dB lower than the VCO due to the divide-by-2 divider operation, which is showed in Fig. 8. Since the measurements are made on only one port of the differential ports. If the differential outputs are got, more than 3dB phase

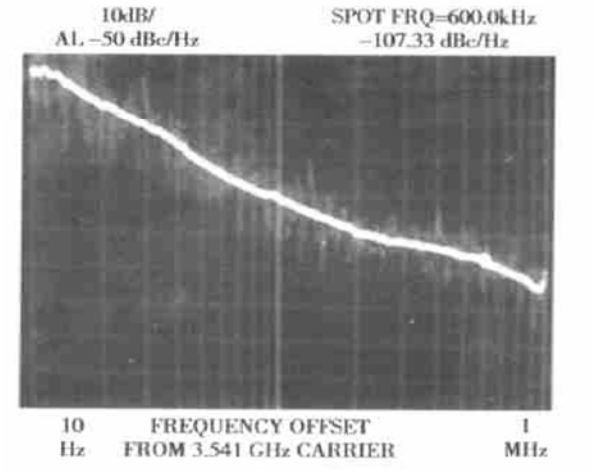


Fig. 7　Phase noise for 3.54GHz VCO

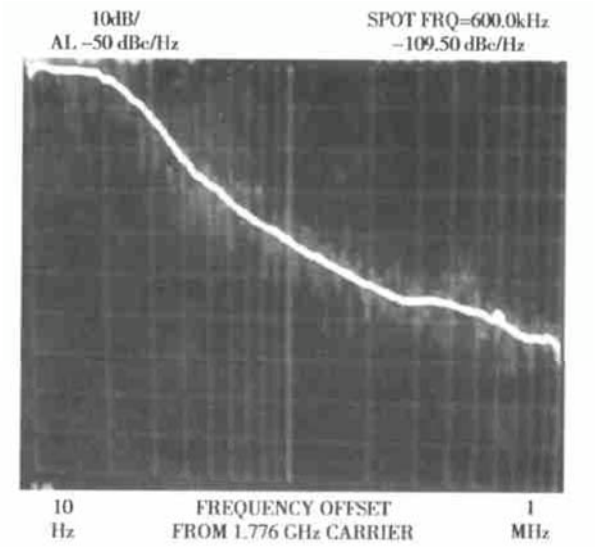


Fig. 8　Phase noise for ILFD units

noise lower could be expected.

## 4 Conclusions

The paper presents an integrated low-power CMOS VCO and its divide-by-2 dividers for WLAN transceivers. The circuit is implemented in a 0.18μm CMOS process. Measurements show the proposed circuit could produce 3.6/1.8GHz dual band LO signals with a wide tuning range and low phase noise. 1.8GHz LO signals are quadrature. It consumes 5mA at $V_{DD}$= 1.5V. The size of die area is only 1.0mm×1.0mm.

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# 集成低功耗 CMOS 压控振荡器及其二分频器


池保勇 石秉学

(清华大学微电子学研究所 100084, 北京)



**摘要**: 实现了应用于无线局域网收发机的集成低功耗 CMOS 压控振荡器及其二分频器. 压控振荡器是由在片对称螺旋型电感和差分容抗管组成的 LC 负阻型振荡器, 而二分频器采用了 ILFD 结构. 由于采用了差分 LC 元件和 ILFD 技术, 整个电路的功耗很低. 该电路已经用 0.18μm CMOS 工艺实现. 测试结果表明该电路能产生低相位噪声的 3.6/1.8GHz 双带本振信号, 并具有很宽的可控频率范围. 当电源电压为 1.5V 时, 该电路消耗了 5mA 的电流. 芯片面积为 1.0mm×1.0mm.



**关键词**: 压控振荡器; 无线局域网收发机; 二分频器

**EEACC**: 1230B; 7250E

**中图分类号**: TN752 **文献标识码**: A **文章编号**: 0253-4177(2002)12-1262-05



池保勇 男, 博士研究生, 研究方向为模拟和射频前端电路设计.

石秉学 教授, 博士生导师, 研究方向包括数模混合信号设计、人工神经网络和模糊逻辑的 VLSI 实现、DC-DC 变换器和射频电路设计技术.


2002-06-13 收到, 2002-08-15 定稿