第 23 卷第 12 期　　半 导 体 学 报　　Vol. 23, No. 12
2002 年 12 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Dec., 2002

Structure Design Considerations of a Sub-50nm Self-Aligned Double-Gate MOSFET*

Yin Huaxiang and Xu Qiuxia

(*Microelectronics Research & Development Center, The Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A comprehensive way to design a sub-50nm SADG MOSFET with the ability of being fabricated by improved CMOS technique is described. Under this way, the gate length and thickness of Si island of DG device show many different scaling limits for various elements. Meanwhile, the spacer insulator shows a kind of width thickness on device drain current and circuit speed. A model about that effect is developed and offers design consideration for future. A new design of channel doping profile, called SCD, is also discussed here in detail. The DG device with SCD can achieve a good balance between the volume inversion operation mode and the control of V_{th}. Finally, a guideline to make a SADG MOSFET is presented.

Key words: double-gate MOSFET; structure design; sidewall effect; SCD
EEACC: 2560B; 2560F; 2560A
CLC number: TN32　　**Document code**: A　　**Article ID**: 0253-4177(2002)12-1267-08

1 Introduction

The double-gate MOSFET (DG MOSFET) is thought as the best to overcome those scaling limits in the nanometer range[1]. DG MOSFET with two gates controlling a single conduction channel (named as Si island) shows many advantages[1]. Normally, it is very difficult to employ the technigue of the current process in mainstream to produce a qualified DG MOSFET. However, there are still some successful cases reported, such as FinFET[2], SSFG[3], VRG[4], DELTA and GAA etc. These device structures can be called self-aligned double gate (SADG) MOSFET for the self-aligned channel in process.

People have done many theory analysis for the DG MOSFET, such as saturation current mode[5], the most important characteristics—— "volume inversion" operation mode[6], prediction to its threshold voltages and sub-threshold swing[7], guideline to scale DG MOSFET[7,8], thickness effects of Si island[9]. These authors usually avoided introducing actual consideration of process for a compact theory analysis. In this paper, we present a comprehensive way to design a sub-50nm self-aligned double-gate MOSFET for fabrication. Here, we firstly set a sight of the technique limits and their effects on an ultra-small DG device. The optimizations of device parameters, including gate length, thickness of Si island, thickness of spacer insulator and channel doping, etc., were performed with the assessment of device performance and practical process conditions. We investigated the thickness of sidewall oxide for its effects on the performance of the SADG MOSFET, which has not been discussed in other

* Project supported by National Natural Science Foundation of China(No. 60176010) and State "973" Project
Yin Huaxiang male, PhD candidate. His work focuses on the ultra-small MOS device with new structure.
Xu Qiuxia female, professor. Her current research includes fabrication of sub-50nm MOSFET and process.
Received 28 March 2002, revised manuscript received 4 July 2002

papers. A new channel doping profile in the thin Si island is also presented to balance the volume inversion operation mode and the control of threshold voltage. Finally, we offered a guideline to make a SADG MOSFET.

2 Device structure

First of all, we design a type of device structure, which is one of SADG structures. As the geometry design and process integration of a DG MOSFET are very complicated, this practical structure should not be discussed here. This paper only covers the device parameter's choice during designing a SADG MOSFET. Fig. 1 shows the scheme of a device structure model which can symbolize our practical SADG MOSFET structure for the analysis. The device simulation is performed on the 3D device simulator, DAVINC4.0 and the structure is constructed on a solid coordinate system as shown in Fig. 1. The main device parameters of a SADG device include gate length (L_G), thickness of gate dielectric (T_{ox}), thickness of Si film (T_{Si}), thickness of spacer insulator (T_{SG} and T_{GD}), lateral diffusion length ($X_{S,D\text{-}ext}$) of source/drain in the channel, and profile of channel doping (N_{ch}), gate electrode material etc.

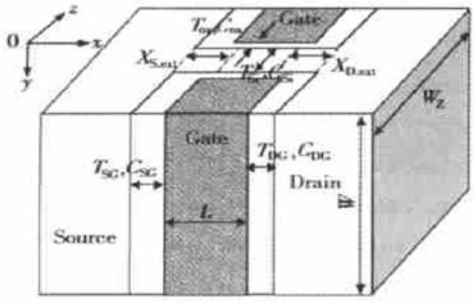

Fig. 1 Model of simulated SADG device structure

3 Gate length scaling limit of DG MOSFET

Which generation should we replace the SG structure for DG structure? The roadmap[10] of Semiconductor Industry Association has indicated that it come into true when the L_G scaling to 20nm. That consideration mainly based on the requirement of IC integration. On the other hand, theory analysis shows the nearly infinite bound to L_G of DG device[8]. Actually, the limit of gate (or channel) length in the DG MOSFET shows different ways. Retarding SCE of super deep sub-micron device during scaling is the primary purpose that we substitute SG with DG structure. SCE of SG device is determined by many elements, including T_{ox}, L_G, depth and lateral abruptness (LA) of S/D junction, channel-doping profile. Optimizing the value of these parameters can improve SCE. Unfortunately, there are some "wallboards" of these parameters, which have no manufacturable solutions to break through with current technigue. According to the roadmap[10], we have to fix $T_{ox} \geqslant 1.5$nm, junction abruptness $\geqslant$3nm/dec for following analysis. At the left axis of Fig. 2, the simulated data of the max T_{Si} to keep V_{th} roll-off< 0.05V as function of L_G shows the lower limit of L_G decided by SCE (excluding the QM effect on V_{th}). Under the same condition of channel doping, although the DG device shows much better SCE immunity than that of the SG device[8], the DG with low channel doping can not keep small V_{th} roll-off as L_G< 50nm yet. One solution is increasing the channel doping to some level, as the second curve shown in Fig. 2, where increasing UCD concentration can enlarge the limited range. The other solution is employing a thinner Si island, which is to be discussed in detail in next section.

Besides SCE, there are some other elements to determine the range of actual gate length during manufacturing a DG MOSFET in Fig. 2. First, the resolution of lithography and etching are the basic elements to be considered. With the best available technigue, the finest line width for device fabrication is about 20nm (EB and hard mask technigue). Next, as the channel of DG device is accustomed to be lightly uniform doping (UCD)[2~6] for satisfying volume inversion mode and high carrier mobility,

the dopant lateral diffusion length ($X_{S,D\text{-}ext}$-$T_{S,DG}$) in the heavy doping Source/Drain should be the second consideration. ($X_{S\text{-}ext}$-T_{SG}) and ($X_{D\text{-}ext}$-T_{DG}) are decided by the lateral abruptness (LA) for Source/Drain doping, whose minimum value is 3nm/dec now[10]. When the $T_{S,DG}$ is fixed. $X_{D\text{-}dep}$ is the thickness of drain depletion layer and it is very small under the control of double-gate, so the L_G should be nearly twice of ($X_{S,D\text{-}ext}$-$T_{S,DG}$). The limits of lateral diffusion length of S/D under different channel are also presented here. Third, the relation between fluctuation of gate threshold voltage (delta V_{th}) and gate length is illustrated at the right axis of Fig. 2, which is derived from the equation (delta V_{th}) = qC_{ox}^{-1} ($T_{Si}N_{ch}$/3LW)$^{1/2}$[8]. Although the QM effect may modify the distribution of carriers and potential and the carriers transporting in the channel[8~11], it could take a key effect only as device size scaling down to 10nm. So the L scale limit decided by QM effect is beyond our design consideration. In summary, the minimum L in our device design is 20nm.

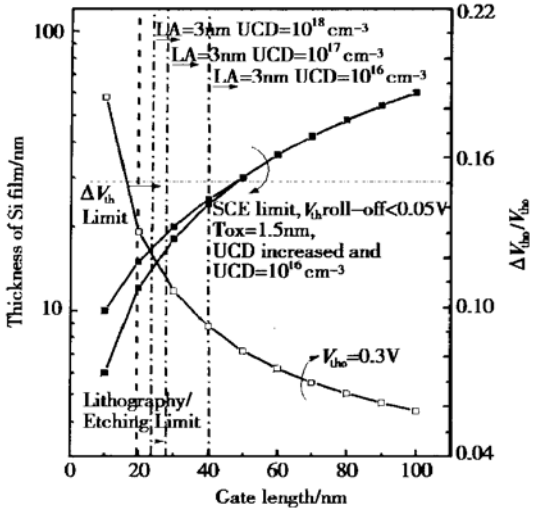

Fig. 2　Various gate length scaling limits for SADG MOSFET

4　Design consideration of T_{Si}

Wong[7] has predicted the T_{Si} should be less than 1/4L_G to keep SCE small. The SCE limit curve in Fig. 2 illustrates the max T_{Si} to keep V_{th} roll-off < 0.05V for different L_G and testifies his theory. In his model, the channel is uniformed for doping and fixed at a low doping level. So these curves also determine the upper limit of T_{Si}. For L_G = 20nm DG device with UCD = 1×10^{16}cm^{-3}, T_{Si} should be less than 10nm. Actually, this "ideal" structure can not be totally realized because of too thin silicon island and the great lateral diffusion from S/D. Then, the limit of T_{Si} is also affected by the resolution of lithography/etching (it can be a little smaller than the resolution of lithography because of etching of the scarified oxide).

The functions of inversion carriers and potential distribution as different T_{Si} of double-gate MOSFET are shown in Fig. 3. As T_{Si} scaling, the carrier's concentration in the Si film increases greatly and the whole Si film is under a stronger volume inversion mode (the concentration of inversion electrons of the whole Si film is larger than

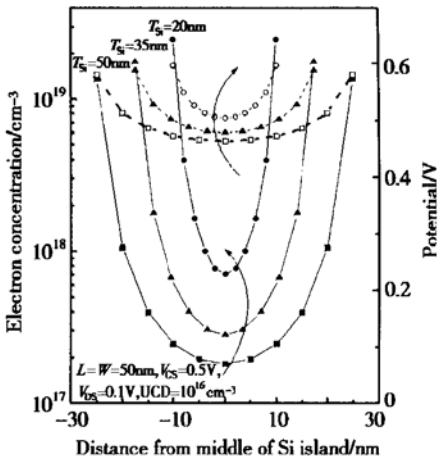

Fig. 3　Simulated data of electrons concentration and potential distribution cross the Si island of SADG MOSFET with different T_{Si}

N_{ch}), so as to get greater drain current for the same device width. However, if the gain from volume inversion can not compensate with the loss of total drain current caused by the smaller area of the Si film in a specific SADG device structure, continued decreasing of the T_{Si} means nothing. The drain current of device decides the lower limit of T_{Si}. As a

result, the satisfaction of T_{Si} is 10~ 50nm according to different channel doping profile.

5 Design consideration of $T_{SG/GD}$

Thickness ($T_{SG/GD}$) of spacer insulators, which is used to isolate double gates from source/drain in the SADG structure, will take more important effect on device performance. First, $T_{SG/GD}$ decides the value of parasite capacitance ($C_{SG/GD}$) between gates and source/drain. Second, it changes the metallurgical length (L_M) of device's gate under a fixed channel doping profile and lateral abruptness of S/D doping. If we have L_M equal to L_G via other hands, $T_{SG/GD}$ will affect the S/D series resistance. The device simulator DAVINC4.0 cannot determine the value of $T_{SG/GD}$ and the relation between them and other parameters. We adopt the way of theory analysis to realize those intentions.

From the Poisson's equation, drift-diffusion equation, and conventional surface channel theory, an equation describing the drain current of DG MOSFET near drain reign with carriers velocity saturation effects is obtained[5]:

$$I_{DS} = 2W\upsilon_{sat}C_{ox}\frac{(V_{GS} - V_{th})^2}{V_{GS} - V_{th} + \alpha E_{sat}L} \qquad (1)$$

where $\alpha \approx 1 + \frac{3T_{ox}}{4T_{Si}}$, υ_{sat} refers to the saturation velocity of channel carriers above saturation electrical field E_{sat}. E_{sat} can be expressed as $E_{sat} = (0.5\times(V_{GS} + V_{th})C_{ox} + qN_AT_{Si})/\epsilon_{Si}$ in the DG MOSFET. V_{th} represents the threshold voltage of surface channel and is given by:

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_{ch}T_{Si}T_{ox}}{2\epsilon_{ox}} \qquad (2)$$

where $\frac{qN_{ch}T_{Si}^2}{8\epsilon_{ox}} \leqslant 2\phi_B$, V_{FB} is the flat-band voltage. ϕ_F is the Fermi-potential in the surface of Si island. ϕ_B is the potential in the mid-channel.

L in Eq. (1) is L_M, which is defined as the space between source and drain junction. In a SADG structure as shown in Fig. 1, normally, the channel is a uniform doping with a low concentration and so there is no self-aligned S/D extension. The device forms S/D area after the spacer insulator has been implemented. As a result, L_M can be expressed as: $L_M = L_G + 2T_{SG/GD} - X_{S\text{-}ext} - X_{D\text{-}ext}$. When we have L_M nearly equal to L_G by the technical ways, the $T_{SG/GD}$ has the same value with $X_{S\text{-}ext}$ or $X_{D\text{-}ext}$.

Equation (1) does not include the series resistance effects in the source and drain. We use the equivalent circuit model modifying the V_{GS} and V_{DS}: $V'_{DS} = V_{DS} + I_{DS}(R_S + R_D)$, $V'_{GS} = V_{GS} + I_{DS}R_S$.

New line where R_S-R_D represents the equivalent series resistance of source-drain. So the effective transconductance in the device is given by:

$$g^*_{ms} = \frac{\partial I_{DS}}{\partial V_{GS}}\Big/\frac{\partial V'_{GS}}{\partial V_{GS}} = \frac{g_m}{1 + g_mR_S} \qquad (3)$$

where $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$.

The total source-drain resistance ($R_{S\text{-}D}$) in the SG MOSFET is composed of four parts: the accumulation-layer resistance (R_{ac}), the effective spreading resistance (R_{sp}), the source or drain sheet resistance (R_{sh}) between the junction depth and contact reign, and the contact resistance (R_{co}). In the DG MOSFET with a volume inversion mode, R_{ac} and R_{sp} are not exist. We will integrate a silicide process and omit the effect of R_{co}. Then, R_{sh} takes the most important effect and $R_{S\text{-}D}$ is decided by resistance of the source-drain extension reign, which is a function of $X_{S\text{-}ext}$ or $X_{D\text{-}ext}$ and R_{sh}.

Figure 1 also shows various capacitances in the device. Gate capacitance (C_G) and Si island capacitance (C_{Si}) are intrinsic capacitance; the overlap capacitance between gate and source (C_{SG}), drain (C_{GD}) and source-drain junction capacitance (C_j) are parasitic capacitance. C_G, C_{Si}, C_{SG}, and C_{DG} can be expressed as: (1) $C_{SG,GD} = \epsilon_{ox}WW_Z/T_{SG,GD}$; (2) $C_G = 2WL\epsilon_{ox}/T_{ox}$; (3) $C_{Si} = WL\epsilon_{Si}/T_{Si}$.

The intrinsic gate delay of a MOSFET can be estimated by $\tau_i = C_Gg^*_m$. However, the basic switching characteristics of a CMOS inverter should include the total capacitance effects in the input and output port. If the load capacitance is zero, the propagation delay of one-stage inverter is $\tau_p = R_{sw}$

(C_{in}+ C_{out}). R_{sw} represents the switching resistance in the channel. We assume PMOS and NMOS to be identical. R_{sw} in the DG MOSFET can be expressed as

$$R_{sw} = \left[1 \Big/ \frac{\partial I_{DS}}{\partial V'_{GS}} \right] + R_S + R_D \qquad (4)$$

Input capacitance (C_{in}) consists of C_G, C_{Si}, C_{SG}, and C_{GD}. Output capacitance consists of the drain junction capacitance ($C_{j\text{-}D}$) and C_{GD}. In this analysis, $C_{j\text{-}D}$ can be omitted for the very small contact area of drain junction with channel in the DG MOSFET.

Figure 4 shows the calculated results of τ_p, τ_i vs $T_{SG,DG}$ in the SADG MOSFET. τ_i represents a intrinsic parameter of a MOS device and can be

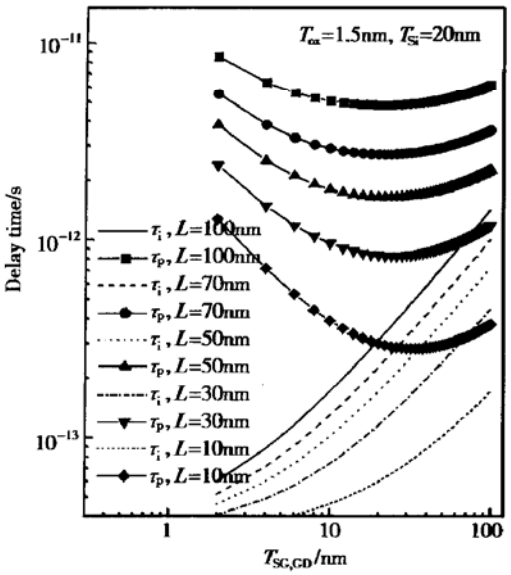

Fig. 4　τ_p, τ_i-$T_{SG,GD}$ characteristics in the SADG MOSFET

scaled down as gate length. For a device, especially a lightly doped DG MOSFET, the parasitic series resistance will take more effects on the device's performance than the parasitic capacitance induced by the sidewall oxide. One can also design a thinner (< 30nm) sidewall oxide in the ultra-small DG MOSFET. However, the propagation delay (τ_p) of one-stage inverter integrated by these devices shows different characteristics. If the value of $T_{SG,DG}$ turns to smaller, the parasitic C_{GS}, C_{DG} become much larger and make τ_p increasing greatly even the improvement of g_m^* can not offset its degrading. τ_p has a minimum value as $T_{SG,DG}$ scaling down. One can optimize the value of $T_{SG,DG}$ for designing a DG MOSFET. Using our physical model, the best $T_{SG,DG}$ for L = 10, 30, 50nm DG MOSFET are 35, 30 and 22nm, respectively. Simultaneously, the gradient of τ_p to $T_{SG,DG}$($\partial\tau_p/\partial T_{SG,DG}$) around the peak point to the right side is smaller than that of the left. So we can make a some larger $T_{SG,DG}$ for the technical reason and keep the discrete effect of $T_{SG,DG}$ caused by the practical process bias is small.

6 Channel doping and gate material design

Figure 5 shows different channel doping profile cross the silicon island. Uniform channel doping (UCD) is the normal choice[2~6] for DG MOSFET because of the formation of volume inversion, higher carrier mobility and less ΔV_{th} (V_{th} roll-off) for the less channel dopant. Unfortunately, uniform doping with low doping level will limit the scaling

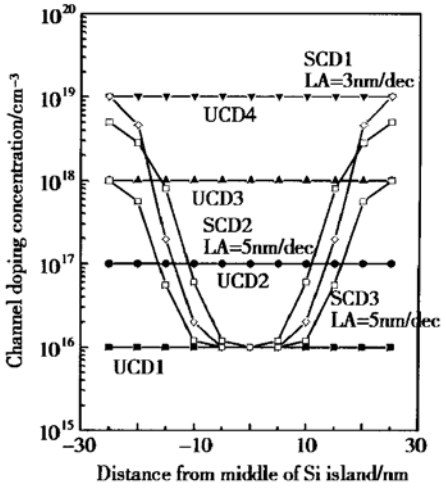

Fig. 5　Simulated data of different channel doping profile cross Si island (z axis)

of L_G, which has been discussed above. Second, such doping will force the threshold voltage into very low, even negative, in the DG MOSFET. Although increasing the channel doping concentration is a potential solution, it makes the inversion carri-

ers in silicon island decreased greatly and consequentially the drive current turns smaller. To achieve a small ΔV_{th} and better drive capability, we designed a new channel doping profile as shown in Fig. 6. The new channel doping is named as "scotia" channel doping (SCD) (Formed by the large tilt implantation). It is decided by the peak concentration (N_p) along the surface of Si island and the lateral diffusion abruptness (LA) of dopants.

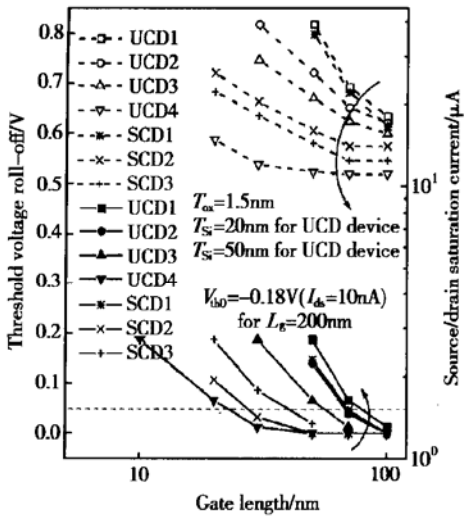

Fig. 6 Threshold voltage roll-off (left axis, delta (V_{th}) = V_{th} - V_{th0}, V_{th0} = - 0.18V when L_G = 200nm) and Source/Drain saturation current (right axis, I_{DS-sat}, V_{GS} = 0.5V, V_{DS} = 1V, T_{Si} = 20nm for UCD NMOS device, T_{Si} = 50nm for SCD device) as function on L_G of SADG device

Figure 6 shows the dependence of ΔV_{th} and $I_{ds,Sat}$ density on L under different channel doping level. The V_{th} roll-off of the SADG nMOSFET for UCD (1, 2) is very large. In fact, the V_{th} (it is defined V_{GS} as I_{DS} = 100nA/μm for nanometer device) of device with that doping is minus and I_{off} (V_{GS} = 0V) is very large and to consume too much extra power in the circuit. Changing the gate material and doping type is the normal way to solve this problem. The materials replacing poly-silicon gate are mid-gap material such as W, TiN and GeSi etc or the dual metal gates such as Ta, $MoSi_x$, Zr for nMOS and Pt, Ru, Ni, Co for pMOS. They can keep V_{th} symmetrical between pMOSFET and nMOSFET and shift it to a reasonable level easily. In this case, the inversion carrier's distribution cross Si island is a little different from that of UCD device with doped poly-Si gate, as shown in Fig. 7. The peak of carrier concentration is at the middle of Si island and makes the MOSFET closer to a bulk-effect device than a surface device, which means higher drive current.

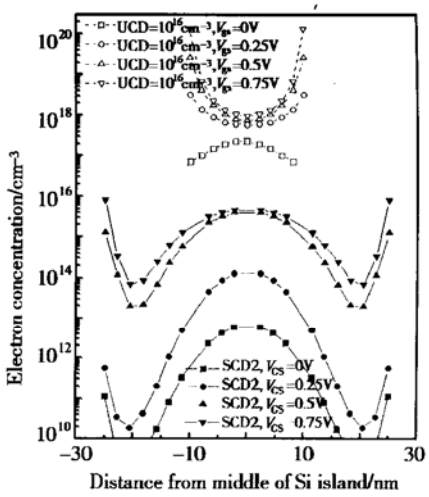

Fig. 7 Distribution of electrons' concentration cross the Si island of SADG MOSFET with different doping profile and midgap gate

With SCD doping, the device can achieve the similar result to that of metal gate. Fig. 6 also shows the characteristics of ΔV_{th} and $I_{ds,Sat}$ versus L in the SADG MOSFET with various SCD doping. The SCD can modify V_{th} above zero while we choose a proper doping condition. Simultaneously, the I_{DS-Sat} degradation for the higher surface concentration in the SCD is much smaller than that of UCD with the same concentration. The reason is that the doping concentration at the middle of Si film is small, which keeps the volume inversion still working. The second reason is that the surface scatter effect still makes little effect on the drain current. Figure 7 shows the distribution of electrons' concentration cross the Si film with different channel doping dose and mid-gap gate. The distribution curve of SCD under 0.5V gate bias is strange and very different from that of other way

of channel doping. But at the middle of Si film, device of SCD has the similar volume inversion mode as that of UCD under zero or tiny bias. Fig. 8 shows the changing of electrons' concentration with the V_{GS} for both UCD and SCD structure. Under a larger bias, SCD device shows different characteristics from that of UCD. The inversing electrons concentration in the middle for UCD has the nearly same concentration as that of SCD around surface; by contrast, the UCD device has the reverse characteristics.

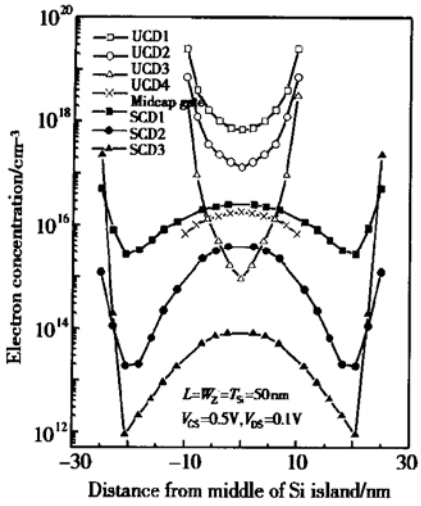

Fig. 8　Distribution of electrons' concentration cross the Si island of SADG MOSFET under different V_{GS}

7　Conclusion

It is apparent that the scaling progress of SG MOSFET can not continue in the several years and the DG, especially SADG structure is the most promising for the post-CMOS era. We presented a consideration of synthesizing the theory analysis, 3D device simulation and process considerations to design a sub-50nm SADG MOSFET for fabrication. Our final optimized results are summarized in Table 1. With different gate length, device needs corresponding structure and process parameters for better device performance and manufacturable feasibility. The thickness of spacer insulator will take more effect on SADG structure than that of normal device and should be optimized carefully. The "scotia" channel doping can modify V_{th} well as the device using the metal gate, high concentration UCD and ultra-thin Si island. Simultaneously, it may produce nearly the same drain current and is to be a preferable choice to make an actual device without introducing new process.

Table 1　Optimized device parameters for a SADG MOSFET

Gate length/nm	50	30	20	50
T_{ox}/nm	1.5~ 2.0	1.5~ 2.0	1.5~ 2.0	1.5~ 2.0
T_{Si}/nm	20	10	10	50
$T_{SG,GD}$/nm	30~ 50	30~ 40	30	30
Channel doping	UCD1	UCD2	UCD3	SCD2
Gate material	Metal	Metal	Metal	Poly-Si

References

[1] Wong H S P, Frank D, Solomon P M, et al. Nanoscale CMOS. Proc IEEE, 1999, 87(4): 537

[2] Huang X J, Lee W C, Kuo C, et al. Sub 50nm FinFET: PMOS. Proc IEDM, 1999: 67

[3] Lee J H, Taraschi G, Wei A, et al. Super self-aligned double-gate (SSDG) MOSFETs utilizing oxidation rate difference and selective epitaxy. Proc IEDM, 1999: 71

[4] Hergenrother J M, Monroe D, Klemens F P, et al. The vertical replacement-gate (VRG) MOSFET. Proc IEDM, 1999: 75

[5] Wann C H, Noda K, Tanaka T, et al. A comparative study of advanced MOSFET concepts. IEEE Trans Electron Devices, 1996, 43(10): 1742

[6] Balestra F, Cristoloveabu S. Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance. IEEE Electron Device Lett, 1987(8): 410

[7] Yan R H, Ourmazd A, Lee K F. Scaling the Si MOSFET: from bulk to SOI to bulk. IEEE Trans Electron Devices, 1992, 39(7): 1704

[8] Wong H S, Frank D J, Solomn P M. Device design consideration for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25nm channel length generation. Proc IEDM, 1998: 407

[9] Majkusink B, Janik T, Walczak J. Semiconductor thickness effects in the double-gate SOI MOSFET. IEEE Trans Electron Devices, 1998, 45(5): 1127

[10] Semiconductor Industry Association (SIA). The national technology roadmap for semiconductors (NTRS). San Jose, CA 95129, 2001

亚 50nm 自对准双栅 MOSFET 的结构设计*

殷华湘 徐秋霞

(中国科学院微电子中心, 北京 100029)

摘要: 描述了一种用综合性方法设计的亚 50nm 自对准双栅 MOSFET, 该结构能够在改进的主流 CMOS 技术上实现. 在这种方法下, 由于各种因素的影响, 双栅器件的栅长、硅岛厚度呈现出不同的缩减限制. 同时, 侧面绝缘层在器件漏电流和电路速度上表现出特有的宽度效应. 建立了关于这种效应的模型, 并提供了相关的设计指导. 另外, 还讨论了一种新型的沟道掺杂设计, 命名为 SCD. 利用 SCD 的 DG 器件能够在体反模式和阈值控制间取得较好的平衡. 最后, 总结了制作一个 SADG MOSFET 的指导原则.

关键词: 双栅 MOSFET; 结构设计; 侧墙效应; SCD

EEACC: 2560B; 2560F; 2560A

中图分类号: TN32 **文献标识码**: A **文章编号**: 0253-4177(2002)12-1267-08

* 国家自然科学基金(批准号: 60176010)和国家"973"资助项目

殷华湘 男, 博士研究生, 研究方向为超小尺寸新结构 MOSFET 的设计与制作.

徐秋霞 女, 研究员, 当前研究方向为亚 50nm 的 MOSFET 制作和工艺技术.

2002-03-28 收到, 2002-07-04 定稿