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Monolithical Integrated CMOS Injected Synchronized Ring VCO for SDH STM-16 Systems*

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Abstract: Oscillator IC technique is developed by combining injecting synchronization technique with a ring VCO. Using the technique, a novel 2.488GHz of monolithical integrated injected synchronized ring VCO (ISRVCO) is realized in a standard 0.25μm CMOS process. The ISRVCO is characterized by the following performances: -100dBc/Hz@1MHz at free running frequency, -91.7dBc/Hz@10kHz when injection is locked. With the 3.3V of power supply, the tuning range is 150MHz and the locking range is 100MHz with 50m$V_{p\text{-}p}$ signal injection.

Key words: VCO; PLL; CRC; injection synchronization; optical transmission systems
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1 Introduction

As tele- and data-communications are rapidly developing, optical transmission systems are widely implemented. The data speeds of the systems are higher and higher. To meet these demands, higher-level of synchronous digital hierarchy (SDH), such as STM-16 at 2.5Gbit/s, has been used for the backbone network. Data signal should be regenerated. For the data regeneration, a clock recovery circuit (CRC) should be utilized and VCO is the key component of CRC in the optical transmission system. Due to the requirements of high frequency, low-phase noise and the poor quality factor of the resonant tank, monolithical integrated VCO is very challenging. And a high-Q phase locked loop (PLL) without frequency acquisition loop using normal VCO suffers from instability caused by the relative narrow locking range.

The paper presents an ISRVCO fabricated in 0.25μm standard CMOS technology and to be used for SDH systems at the level of STM-16. Based on a ring VCO, injecting synchronization technique has been introduced. Using such a VCO, the narrow locking range of PLL in CRC can be resolved. Details of circuit design and measured results will be given.

2 ISRVCO topology

As shown in Fig. 1, ISRVCO includes 4 stages, which composed of one sum and three narrowband amplifiers. The stage 4 was chosen to ensure that the phase shift caused by the total delay of all amplifiers is equal to $2m\pi$ with $m=1, 2, 3\cdots$ at the operational frequency. The summing amplifier is inserted at the front of the ring oscillator to real-

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ize the injection function by adding the injection signal with the oscillation signal. It can be considered as two pairs of parallel-connected current amplifiers with a common LC resonator as loading circuit. The other three stages are differential amplifiers with the same structure. A single-tuned LC resonator filter was served as load for each amplifier.

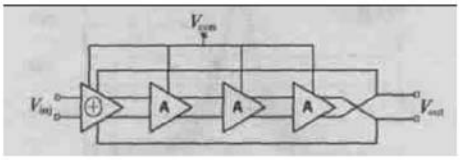

Fig. 1　Block diagram of the injected synchronized ring oscillator

The centre frequency of all resonators was specified identically to increase the open-loop quality factor (Q) rapidly, considering the poor Q of on-chip CMOS resonator due to the substrate loss. It meets the required noise filter performance in the injection application, and better phase noise performance than that of normal ring VCO[1] was achieved. Meanwhile, it has good injecting locking characteristic. Combining this ISRVCO with a high-Q PLL, an injection-synchronized phase-locked loop (ISPLL) was formed[2~5]. Under the activations of both injecting synchronization and PLL, a wider locking range and a better loop phase noise were obtained instead of a complex auxiliary frequency acquisition loop in CRC. Certainly it can be used as a normal VCO.

3　Inductor and varactor designs

Inductor and varactor are not available in the technology library from the foundry. An on-chip square spiral is simulated by momentum electromagnetic field analysis of the CAD-tool ADS. Due to an increase of the loss caused by the skin effect at the high frequency, the width of the inductor traces cannot be made extremely large. The spiral must not be filled up with conductor traces up to the middle of the coil. The innermost turns contribute only a small amount of inductance, but their high-resistance increases enormously due to eddy-currents caused by the magnetic field of the outer turns[6].

The traces spacing, width, and inner dimension of the optimized inductor are 2, 10, and 120μm, respectively. The inductor was made of the top metal (Metal 5). At the operational frequency for 2.488GHz, we obtained an inductance for 10nH, a quality factor for 6, and a self-resonant frequency for about 4.7GHz.

To build a varactor, we have connected gate, source, and drain of a pMOS as one terminal, and use n-well as the other terminal. All of the junction capacitances of source/drain to substrate and MOS capacitance of pMOS are used as varactors. Thus the varactor dimension is kept small. The n-well terminal is connected to control electrode so that the n-well to substrate capacitance appears as common-mode and does not affect the tank.

4　Measurement results

The proposed circuit was fabricated in TSMC 0.25μm CMOS process via MOSIS multiproject runs. This process has 1 poly and 5 metal layers.

Figure 2 shows the test box. Printed circuit broad (PCB) is fixed onto the brass box by some screws and the chip is bonded to the micro strips at the center of PCB. Microwave connections (SMA) are set at the edge of the box to input and output signals and connected with measurement instruments.

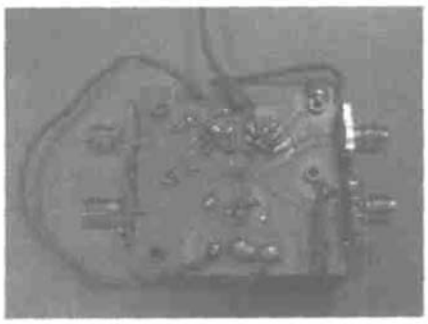

Fig. 2　Photograph of test box

The chip draws 33mA from a 3.3V power supply, 12mA for the VCO core, and 21mA for the input and output buffers. The output buffer is used to drive 50Ω load of the measurement equipment. When measured, one single-ended signal of the differential output is sent into the spectrum analyzer, while the other was terminated with a 50Ω precision load.

The center frequency of the VCO is 2.488GHz (SDH STM-16). The measured tuning characteristic versus control voltage is shown in Fig. 3. Notice that the tuning curve is quite linear, which makes this circuit a good choice for integrating into a CRC. Figure 4 shows the output spectrum of the free running VCO. The phase noise calculated from output spectrum is - 100dBc/Hz@ 1MHz.

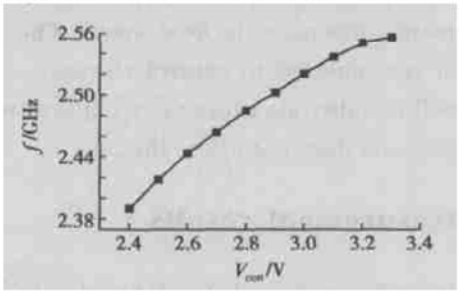

Fig. 3 Measured tuning characteristic of the VCO

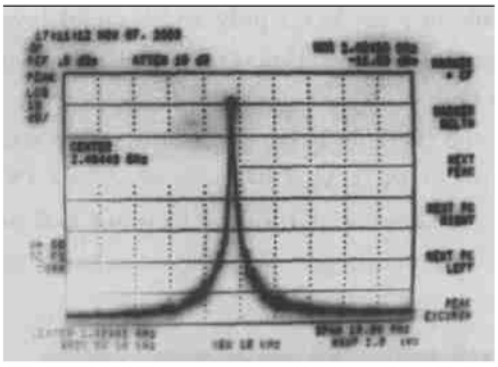

Fig. 4 Measured output spectrum (SPAN 10MHz; VBW 10kHz; Center 2.48GHz)

The injection-locking characteristic was measured. The relationship between locking range and injection power is given in Table 1. The locked output spectrum has better phase noise performance, as shown in Fig. 5. The phase noise is - 91.7dBc/Hz@ 10kHz.

Table 1 Injection locking characteristic

Injection signal amplitude (V_{p-p})/mV	Locking range/MHz
25	49
50	100
100	290

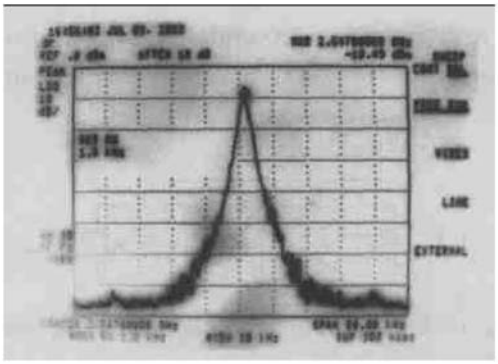

Fig. 5 Locked spectrum at 2.547GHz with 50m V_{p-p} injection

5 Conclusion

A monolithical integrated 2.488GHz CMOS ISRVCO for SDH STM-16 system has been presented. It exhibits a phase noise for - 100dBc/Hz @ 1MHz and a tuning range for 150MHz. The standard frequency, 2.488GHz, can be covered with injection signal amplitude of less than 25mV. And with 100mV of injection signal amplitude, it has a locking range for 290MHz. This circuit can be used as a stand alone VCO or as a building block of clock synthesizer, FM demodulator, and phased arrays.

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SDH 系统 STM-16 速率级 CMOS 注入同步环形振荡器*

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摘要：基于0.25μm CMOS 工艺，通过在环形振荡器的基础上引入注入同步技术，实现了一种新颖的应用于SDH 系统STM-16 速率级的注入同步振荡器. 测试结果表明，该振荡器中心频率为2.488GHz，具有150MHz 的电压调谐范围，相位噪声为-100dBc/Hz@1MHz. 当注入峰峰值为50mV 的信号时，相位噪声为-91.7dBc/Hz@10kHz，并具有100MHz 的锁定范围. 应用这种注入同步振荡器于时钟恢复电路的高 Q 值锁相环时，可以解决窄锁定范围的问题，而无需另加复杂的锁频环.

关键词：压控振荡器；锁相环；时钟恢复电路；注入同步；光纤传输系统

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