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Low Voltage CMOS Gilbert Mixers for Bluetooth Transceiver

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Abstract: Based on the analyses of the reported Gilbert mixers operating at low supply voltage, a down-conversion mixer and an up-conversion mixer for 2.4GHz bluetooth transceiver are presented with the modified low voltage design techniques, respectively. Feedback and current mirror techniques suitable for low voltage operation are used to improve the linearity of the up-conversion mixer, and folded-cascode output stage is adopted to optimize the noise and conversion gain of the down-conversion mixer operating at low voltage. Based on 0.35μm CMOS technology, simulations are performed with 2V supply voltage. The results show that 20dBm third-order intercept point (IIP3), 87mV output signal amplitude are achieved for up-conversion mixer with about 3mA current; while 20dB conversion gain (CG), 6.5nV/ $\sqrt{\text{Hz}}$ input-referred noise, 4.4dBm IIP3 are obtained for down-conversion mixer with about 3.5mA current.

Key words: bluetooth transceiver; low voltage; mixer
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1 Introduction

With the development of wireless communication systems, there is a persistent demand for light, inexpensive, low power, and hand-held terminals. This excited rapid evolution of highly integrated radio frequency (RF) transceiver within CMOS technologies. Being contemporaneous with this evolution is the reduction in supply voltage standards for integrated circuits. Low power and low supply voltage are key issues involved in designing the CMOS RF circuits, and low voltage design idea has been proposed for the RF circuit[1].

Mixer is an essential part of wireless communication systems, which performs frequency translation by multiplying two signals. We introduce the basic design requirements for CMOS mixer used in 2.4GHz bluetooth transceiver. The limitations of reported Gilbert mixer at low supply voltage are analyzed, the modified up-conversion and down-conversion mixers capable to operate with low supply voltage are presented, respectively. Simulations are performed using Chart 0.35μm CMOS technology under 2V supply voltage.

2 CMOS mixer design requirements

Figure 1 shows the typical block diagram of bluetooth transceiver[2,3], which is suitable for low power and high integrity design. Down-conversion mixer employed in the receiver path translates input 2.4GHz RF signal to 2MHz intermediate frequency (IF) signal. Due to the interferers existing

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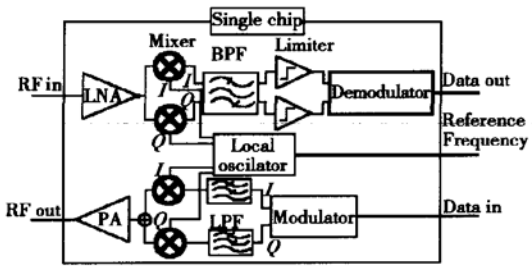

Fig. 1 Bluetooth transceiver architecture

in RF noisy environment in which several powerful radio signals (e. g., GSM or CDMA signals) are present in the proximity of the bluetooth radio, the receiver mixer must be designed to satisfy certain noise and linearity requirements set by the standard so as to detect correctly the desired signal. In the design, the required input-referred noise voltage must be lower than 8nV/ $\sqrt{\text{Hz}}$ and the IIP_3 at least 2dBm with a differential local oscillator (LO) signal amplitude V_{LO} of 300mV. In addition, to reduce the noise contribution from the IF stages followed by the mixer, its conversion gain should be as high as possible, e. g. > 15dB. On the transmit side, mixer upconverts the input 2MHz IF signal to the 2.4GHz RF signal. Unlike in the receiver path, the input IF signal is generated in the transmitter and the signal level is well controlled. So, the goal in the up-conversion mixer design is to realize large output signal amplitude rather than high conversion gain and low noise. In addition, since third-order nonlinearity in the mixer will produce out-of-channel leakage and generate interference in adjacent channels, low distortion is also desired. In this design, the required IIP_3 of the mixer is at least 18dBm, and if the voltage gain of 20dB is assumed in power amplifier(PA), the output signal amplitude of the mixer should be higher than 50mV, while a 0.4V differential IF signal and a 0.3V differential LO signal amplitude are used. Besides performances required above, high port-to-port isolation levels are desired for down-conversion mixer and up-conversion mixer[4].

Although many mixer structures exist and some new ones have recently been proposed[4], the only configuration that fulfills most of the requirements at 2.4GHz is the well-known Gilbert mixer[2,3,5]. Traditional Gilbert mixer is initially designed with bipolar transistor[6], and a CMOS counterpart is shown in Fig. 2. The IIP_3 of this type of mixer is mainly bounded by that of the transconductance stage[4], and more detailed analysis for the conventional Gilbert mixer can be found in Refs. [7, 8], especially about the current-commu-

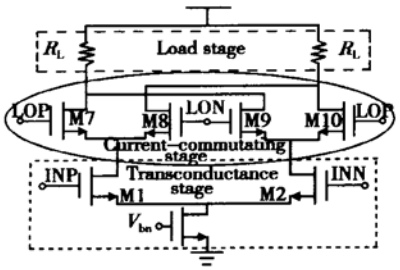

Fig. 2 Conventional double-balance CMOS Gilbert mixer

tating stage design. In the following design, the current-commutating stage will not be further dealt with, and their dimensions have been optimized to minimize their influences on the performance of the mixers. The drawback inherent to the traditional Gilbert mixer is that it needs higher supply voltage because of the stacked transistor configuration. It has been shown that the performance of the traditional mixer degrades dramatically when the supply voltage is reduced[9]. In particular, the dynamic range requirement will become more and more stringent due to the reduced voltage headroom available. Therefore, there is a need for mixer that can operate at low supply voltage (e. g., 2V), and meet the requirements of 2.4GHz bluetooth transceiver.

3 Modified low voltage Gilbert CMOS up-conversion mixer

Since high IIP_3 required by up-conversion mixer, various feedback techniques have been devel-

oped to improve the linearity of the transconductance stage of the mixer, as illustrated in Figs. 3 (a)[10] and (b)[11]. However, with these methods, the mixer cannot work at low voltage (e.g., 2V), when using 0.35μm technologies with threshold voltage of the NMOS and PMOS transistor around 0.65V and −0.85V, respectively. For instance, in Figs. 3(a) and (b), to achieve sufficient voltage swing at the drain of M0 and M3 operating in the saturation region, the dc voltage V_S of these drains

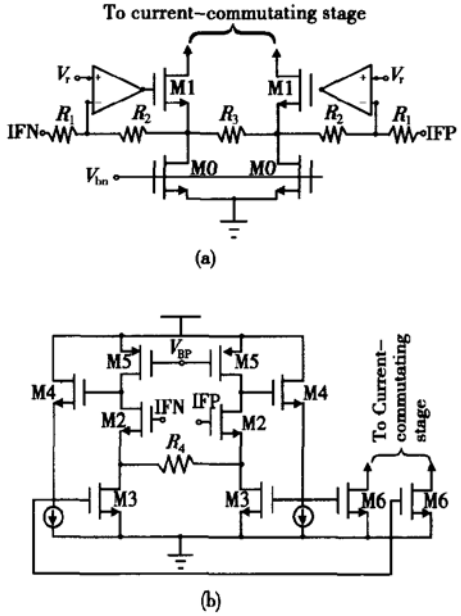

Fig. 3 Modified transconductance stage for up-conversion Gilbert cell mixer by Paolo (a) and Liu (b)

should be kept high enough (e.g., 0.7V) and consequently a high dc bias V_G at the gate of M1 and M2. Assuming a minimum effective gate-source voltage V_{eff} of 0.3V based on the current mirror mismatch consideration[12], the value of V_G should be at least equal to $V_S+V_{eff}+V_{thn}=1.65$V. Considering the body effect of M1 and M2, the value will be further elevated. This limits the available input IF signal range in a low supply voltage system. In addition, in Fig. 3(b), the branch formed by transistors M3~M5 requires a power supply of $2V_{thn}+3V_{eff}$ at least, making the mixer also unsuitable to supplies below 2.2V.

To overcome these limitations, a Gilbert mixer with modified transconductance stage and load stage is proposed, as illustrated in Fig. 4. In this design, the amplifiers A1 and A2 are the main limitations to reducing the supply voltage. However, even the amplifier is implemented using current mirror structure, the mixer can be operated with a supply voltage as low as $3V_{eff}+|V_{THp}|=1.75$V. Due to the low-speed operation, the bias current of A1 and A2 can be very low. A dc offset signal V_{os} between the two amplifiers A1 will cause an extra carrier leakage, and the carrier feedthrough suppression is determined by the ratio of the V_{os} over the input signal. For an offset voltage typically in the order of a few mV, the carrier feedthrough is then higher than 30dB, and satisfies the requirement of transmit spectrum mask.

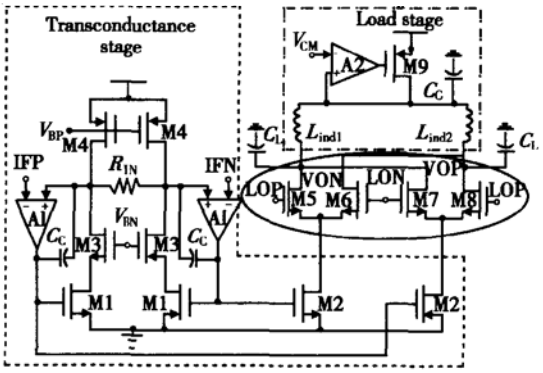

Fig. 4 Schematic of the modified low voltage up-conversion Gilbert mixer

At the transconductance stage, the feedback loop based on the amplifiers A1 regulates the current in transistor M1, so that the variation of differential input IF voltage signal is directly transferred to the resistor R_{in}. The input signal voltage is therefore translated into an input signal current I_{in} so that $I_{in}=V_{in}/R_{in}$. By duplicating the current of M1 by M2, a linear transconductance stage is formed. Capacitor C_c generates Miller compensation for the feedback loop. Because the nonlinearity of the drain current of transistor M1, which is the main nonlinearity in the cascade stage formed by A1 and M1, can be suppressed by increasing the loop gain, the linearity of the current mirror (M1,

M2) itself is the fundamental limitation of linear transconductance stage. This is because the current mirror is outside the feedback loop, and any nonlinearity of the current mirror will directly enter into the transfer function of the transconductance stage. There are two main sources of nonideality, which limit linearity of the current mirror. One is the channel-length modulation error of M1 and M2. This limitation can be reduced to an insignificant level by adopting long channel or cascode transistor (such as M3). According to simulation results, a channel length of 1μm may be proper. The other nonlinearity source comes from mismatches between M1 and M2. In this case, the IIP3 in Amp for current mirror can easily be estimated from the expression

$$I_{\mathrm{IIP3}} = 4\sqrt{\frac{2}{3}} \times \sqrt{\frac{V_{\mathrm{GS1}} - V_{\mathrm{TH1}}}{\Delta V_{\mathrm{TH}}}} I_{\mathrm{Bias1}} \qquad (1)$$

where $\Delta V_{\mathrm{TH}} = V_{\mathrm{TH2}} - V_{\mathrm{TH1}}$, I_{Bias1} is the dc bias current of M1. A good transistor matching (low ΔV_{TH}) requires considerable transistor area[12], so high linearity of current mirror can be achieved by increasing the transistor widths. However, the parasitic capacitance on the source node of the switching pair is increased, leading to a lower pole frequency and ultimately degrading the linearity of the mixer[8]. Thus, the linearity of the current mirror is a tradeoff between the supply voltage (V_{GS}), the pole frequency, and the power (I_{Bias1}). From Eq. (1), it can also be seen that the linearity is independent of the geometric size ratio of M2 and M1. In this design, the choice of the ratio, m ($m = W_2/W_1$ with $L_2 = L_1$), depends on mixer output signal amplitude. Considering the output signal loss caused by the switching pair, an optimum m providing maximum output signal amplitude exist as in Eq. (2):

$$m = \left| \frac{2\pi}{3\sqrt{2}} \times \frac{V_{\mathrm{LO}}}{V_{\mathrm{eff,sw}}} \right| \qquad (2)$$

where we have assumed a simple long-channel transistor model. In fact, because the minimum channel length is chosen for switching transistor, the short-channel model is more valid, and then the actual value of m is lower than predicted by Eq. (2). In addition, the limitation of parasitic capacitance at switching node also results in a smaller value for m, e.g., $m = 2$.

In the bluetooth transmitter path shown in Fig. 1, the PA is integrated on the same chip with the up-conversion mixer. With this highly integrated transceiver architecture, the 50Ω matching is not required at mixer output. However, unfortunately, the gate capacitance of input devices of PA is always very large (e.g., 300fF), and severely limits the output bandwidth of the mixer and thus decreases the output signal amplitude. So, the on-chip inductors L_{ind1}-L_{ind2} are used to tune out the total capacitance associated with the mixer output. In this case, the equivalent resistive load is

$$R_{\mathrm{L}} = R_{\mathrm{s}}(1 + Q)^2 \qquad (3)$$

where R_{s} represents the parasitic resistance of the inductor and Q is quality factor. If $L_{\mathrm{ind1}} = L_{\mathrm{ind2}} = 3.99$nH is chosen, the Q is 6.203, and R_{s} is about 5Ω, then $R_{\mathrm{L}} = 260\Omega$ is obtained. This not only yields higher output voltage swing, but also increases the dc voltage headroom. In addition, to prevent the output RF signal from swinging above V_{dd}, thereby reducing its interference in other parts of the system, the feedback loop composed of A2 and transistor M9 is used to set the output common mode voltage. At the same time, this approach also improves the power supply rejection ratio (PSRR) of mixer and suppresses any residual low frequency signal at mixer output. MOS capacitor C_{G} is added to increase the phase margin of common-mode stability and further keep the connection of L_{ind1}-L_{ind2} virtual ground for RF signal.

4 Modified low voltage Gilbert CMOS down-conversion mixer

For the receiver application, the traditional Gilbert mixer (Fig. 2) with grounded source input transistors is preferred to improve the linearity[13]. In this case, the input signal range is $\sqrt{2}\times$ larger than the differential pair case, and the IIP3 in Volts

for the mixer can be approximated by the following expression using a power series expansion on the I–V relationship of the input transistors:

$$V_{\mathrm{IIP3}} \approx \frac{4}{\sqrt{3}} \times \sqrt{\frac{V_{\mathrm{eff,in}}}{\theta}} \tag{4}$$

where the parameter θ is the normal field mobility degradation factor and $V_{\mathrm{eff,in}}$ is the effective gate-source voltage on input devices M1 and M2.

However, it is difficult to obtain sufficient gain at a low supply voltage after considering many tradeoffs. These tradeoffs can be seen if we write for the mixer conversion gain:

$$G_{\mathrm{c}} = \frac{2}{\pi} g_{\mathrm{m,in}} R_{\mathrm{L}} = \frac{2}{\pi} \times \frac{I_{\mathrm{B,in}} R_{\mathrm{L}}}{V_{\mathrm{eff,in}}} \tag{5}$$

where $g_{\mathrm{m,in}}$ and $I_{\mathrm{B,in}}$ are the transconductance and the dc bias current of either M1 or M2, respectively, and $I_{\mathrm{B,in}} R_{\mathrm{L}}$ denotes the dc voltage drop across the resistor loads. It is immediately apparent that the tradeoffs exist between conversion gain (CG), voltage headroom ($I_{\mathrm{B,in}} R_{\mathrm{L}}$) and linearity ($V_{\mathrm{eff,in}}$). Although extra current sources can be added to transconductance stage to increase the conversion gain[3,11], this is achieved at the cost of the mixer linearity degradation because of the lower dc current through the switching transistors[8]. In fact, due to the existence of output impedance and the parasitic drain-bulk and drain-source capacitance of the extra current source at the source node of switching pair, allowing more RF current provided by the input transistors to be shunted to ground. This approach increases only a small amount of the conversion gain. Moreover, the noise current arising from additional current sources itself directly adds to the RF current signal, thereby increasing the mixer noise.

On the other hand, a mixer loaded with a differential FET resistor and biased with pull-up current sources can decouple the conversion gain from supply voltage, as shown in Fig. 5[13]. The PMOS current sources M7, M8 should be biased at small effective gate-source voltage, $V_{\mathrm{eff,cs}}$, to achieve high output swing at low supply voltage, which however

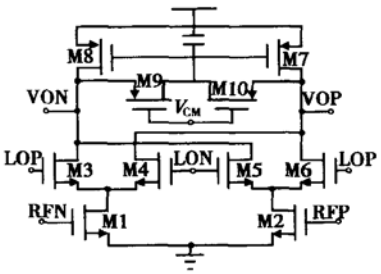

Fig. 5 Rofougaran modified Gilbert cell mixer

enhances their noise:

$$\overline{i_{\mathrm{n}}^2} = 4kT\gamma g_{\mathrm{m,cs}} = 4kT\left(\gamma \frac{2I_{\mathrm{B,in}}}{V_{\mathrm{eff,cs}}}\right) \tag{6}$$

where γ is coefficient of channel thermal noise. Generally, the noise from pull-up current sources dominates total white noise of the mixer. For example, in a mixer biased at 1.3mA, γ of 2/3 and a load of 2kΩ, with input devices biased at 0.3V effective gate-source voltage, and the pull-up current sources at 0.2V, the total white noise referred to the mixer input can be found using the following expression[14]:

$$\overline{v_{i,n}^2} = \frac{8kTR_{\mathrm{L}}}{G_{\mathrm{c}}^2}\left(1 + \gamma\frac{2R_{\mathrm{L}}I_{\mathrm{B,in}}}{\pi V_{\mathrm{LO}}} + \gamma\frac{I_{\mathrm{B,in}}R_{\mathrm{L}}}{V_{\mathrm{eff,in}}} + \gamma\frac{2I_{\mathrm{B,in}}R_{\mathrm{L}}}{V_{\mathrm{eff,cs}}}\right) \tag{7}$$

where the first three terms are due to two load resistors R_{L}, the four switches, and the two input devices, respectively. In the above equation, the magnitude of fourth term is 17.3(about 64% of the total white noise), which is much greater than the other three terms.

From the above discussion, it can be seen that the down-conversion mixer design contains many compromises among conversion gain, linearity, noise, output swing, and the supply voltage. Therefore, a mixer, which gives more design freedom especially at low supply voltage, is desired. For these reasons, a mixer with modified output stage is proposed, as shown in Fig. 6.

The commutated output currents are folded to the load resistors through the cascode transistors M9 and M10. In this case, the impedance at node A (B) is dominated by M9 (M10), and is about $1/g_{\mathrm{m9}}$ ($1/g_{\mathrm{m10}}$). By choosing the size of the devices M9

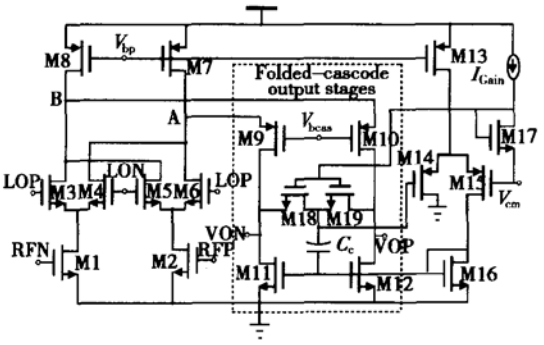

Fig. 6 Schematic of the modified low voltage down-conversion Gilbert mixer

and M10, the impedance can be set very low, leading to a low voltage swing at node A and B. This means that the pull-up current sources can be biased at a much higher $V_{\text{eff, cs}}$, hence its noise can be made much lower according to Eq. (6), breaking the classical tradeoff between the dominated white noise source and the output voltage swing, and resulting in an important extra degree of design freedom. Although the additional noise sources are introduced by transistors M11 and M12, the total white noise contribution from the folded-cascode output stage is still reduced in comparison with the case in Fig. 5 because the current through M11 (M12) can be lowered until minimum satisfaction:

$$I_{11\_12,\min} > \frac{2}{\pi} g_{m,\text{in}} v_{\text{in,max}} \tag{8}$$

where $v_{\text{in,max}}$ denotes the maximum input signal of mixer. For example, for the case in which I_{11_12} = 0.2mA, $V_{\text{eff},7\_8}$ = 0.6V (three times as large as in Fig. 5) and $V_{\text{eff},11\_12}$ = 0.4V, the white noise contribution from output stage can be reduced by about 20%. In addition, with the small dc currents through M11 and M12, high output impedance ($r_o \propto 1/I_{11\_12}$) can be achieved, which means that most of the output currents flow into load resistor and thus the nonlinearity caused by output impedance is reduced. For the same linearity requirement at output node, the load resistance R_L, and hence the conversion gain can be increased, which means that the gain stage[3] following the mixer can be eliminated, and saves the system current. Another important advantage of the folded-cascode output stage may be to allow the designer to realize the dc coupling between the mixer and bandpass filter (BPF) by using the common-mode feedback circuit composed of M13~ M16, and save the areas needed by the ac coupling capacitors used in Ref. [3]. The compensation for the common-mode feedback loop is provided by Cc. If the current sources I_{Gain} and diode-connected transistor M17 are used, the conversion gain can be adjusted on-chip by varying the current I_{Gain}.

5 Consideration of circuit simulation and experimental results

Both circuits are designed using Chart 0.35μm CMOS process. The compensation capacitors in the design are PIP caps, the load capacitors are MIM caps, and resistor model used in the simulation is rpl-res (n^+ poly unsalicided res.). The models and GDS files of RF transistors and inductors are both provided by the foundry. The MOSFET RF model is based on BSIM3v3 MOSFET model and some passive components are added to characterize the parasitic effects in the high frequency range[15].

Simulations are performed under 2V voltage supply, and the results show that the up-conversion and down-conversion mixers including the bias circuits consume 3mA and 3.5mA, respectively, which are very low. To find IIP3 of the up-conversion mixer through a transient simulation, the input IF signal $0.4\sin(2\pi\times 2\text{MHz}\times t) + 0.4\sin(2\pi\times 1.4\text{MHz}\times t)$ and the LO signal $0.3\sin(2\pi\times 2.45\text{GHz}\times t)$ are applied. So, the desired output components are at 2.4486, 2.448, 2.4514 and 2.452GHz, respectively, while the third-order intermodulation products are at 2.4474, 2.4492, 2.4514GHz, and 2.4526GHz, respectively. Combining fast Fourier transform(FFT) analysis, the output spectrum for the up-conversion mixer is displayed in Fig. 7. This simulation shows that the desired amplitude of output signal is about -21dB (i.e., 87mV), and the third-order intermodulation

products is about - 57dB, then it could be deduced that the IIP_3 is at least 20dBm ($IIP_3|_{dBm} = P_{in}|_{dBm} + \Delta P|_{dB}/2$).

The performance of down-conversion mixer is simulated using Cadence Spectre-RF periodic steady-state analysis, which can analyze the noise of nonlinear circuits such as mixers. The result given in Fig. 8 shows that 6.5nV/$\sqrt{\text{Hz}}$ input-referred noise is obtained. From the simulated output file, it can be seen that 42% of total white noise contributed to the folded-cascode output stage. The conversion gain can be found to be 20dB. The IIP3 of 4.4dBm is also illustrated in Fig. 8, which using two RF frequency separated by 3MHz apart.

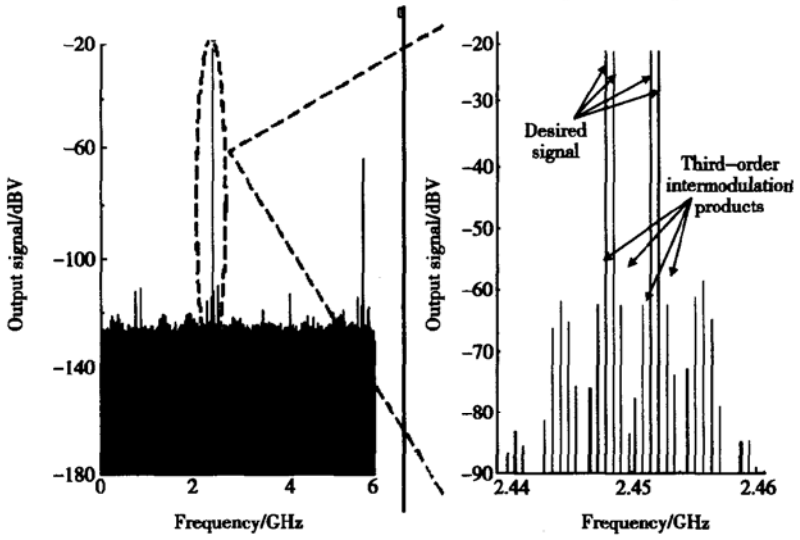

Fig. 7 Output spectrum of the up-conversion mixer

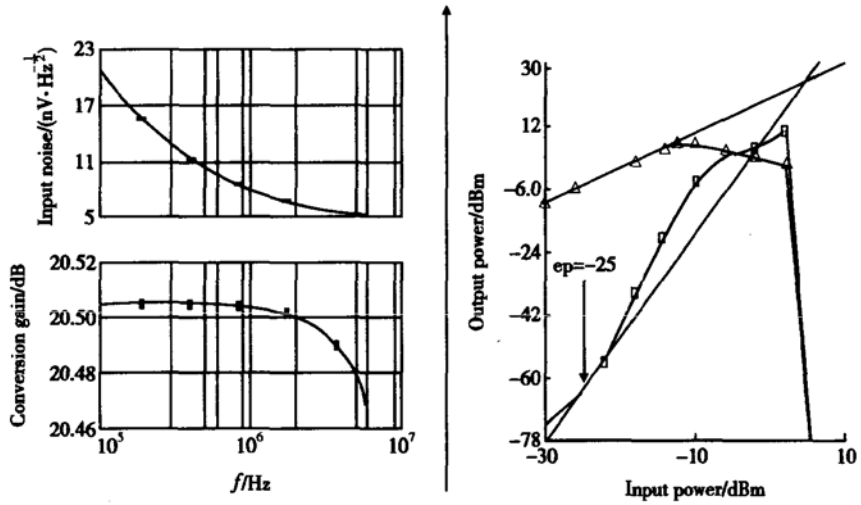

Fig. 8 Input-referred noise voltage, conversion gain and IIP3 of the up-conversion mixer

6 Conclusion

In our work, the up-conversion and down-conversion Gilbert mixers with modified low voltage design techniques are presented. For up-conversion mixer, feedback and current mirror techniques suitable for low voltage operation are used to improve the linearity of the transconductance stage, while the load stage adopts on-chip inductor to increase the output signal amplitude and the voltage headroom. For down-conversion mixer, the folded-cascode output stage is proposed to offer an extra de-

sign freedom, which reduces the noise and increases the conversion gain. Using 0.35μm CMOS technology, simulations are performed under 2V supply voltage. The results show that the performances satisfy the requirements of bluetooth transceiver. Although the design is verified only by simulation, it is believed that the ideas of the low voltage design could be helpful for other designers, and the mixer topologies suitable for low voltage operation would make more robust to technology scaling. For example, for 0.18μm CMOS technology, the modified mixers will be more applicable because the lower power supply voltage is allowed.

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用于蓝牙收发机的低电压 CMOS Gilbert 混频器

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(复旦大学集成电路设计实验室, 上海 200433)

摘要: 对已报道的 Gilbert 混频器工作在低电压时存在的问题进行了分析, 在此基础上, 描述了利用改进的低电压设计技术, 用于 2.4GHz 蓝牙收发机的上混频器/下混频器的设计. 利用适用于低电压工作的负反馈与电流镜技术提高上混频器的线性度; 而通过采用折叠级联输出, 增加了低电压时下混频器的设计自由度, 从而降低了噪声, 提高了转换增益. 基于 0.35μm CMOS 工艺技术, 在 2V 电源电压下, 对电路进行了仿真. 结果表明: 上混频器消耗的电流为 3mA, 输入三阶截距点达到 20dBm, 输出的信号幅度为 87mV; 下混频器消耗的电流为 3.5mA, 得到的转换增益是 20dB, 输入参考噪声电压是 6.5nV/$\sqrt{\text{Hz}}$, 输入三阶截距点为 4.4dBm.

关键词: 蓝牙收发机; 低电压; 混频器

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