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Polarization-Insensitive Silica on Silicon Arrayed Waveguide Grating Design*

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Abstract: A new technology for fabrication of silica on silicon arrayed waveguide grating (AWG) based on deep etching and thermal oxidation is presented. Using this method, a silicon layer is remained at the side of waveguide. The stress distribution and effective refractive index of waveguide fabricated by this approach are calculated using finite element and finite difference beam propagation method, respectively. The results of these studies indicate that the stress of silica on silicon optical waveguide can be matched in parallel and vertical direction and AWG polarization dependent wavelength (PDλ) can be reduced effectively due to side-silicon layer.

Key words: silica on silicon; arrayed waveguide grating; stress; birefringence; polarization dependent wavelength; numerical analysis
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1 Introduction

With the rapid increase of channel counts in dense wavelength division multiplexing (DWDM) systems, integrated arrayed waveguide grating (AWG) devices, especially low loss and high coupling efficiency silica on silicon AWGs, are attractive and essential components for various applications requiring wavelength multiplexing/demultiplexing functions. But a problem remains with its PDλ. It is thought to result from the use of silicon substrate, which upon cooling after the sintering or annealing of the glass layer strains the glass layer because of its different expansion coefficient. This PDλ must be reduced substantially before silica on silicon AWG is practically introduced. Several approaches have been reported for eliminating the PDλ[1~4]. This paper describes a new method for fabricating low PDλ silica-based AWG. Stresses of silica waveguide with a side-silicon layer are examined using finite element method (FEM). At the same time, the effective refractive index are calculated using finite different beam propagation method(FD-BPM). After optimizing the width and depth of side-silicon layer, a polarization insensitive AWG is designed, and output spectra is simulated using single transmission function.

2 Methods for fabrication

The process flow of fabrication for a buried silica on silicon AWG under study is shown in Fig. 1. The first step is to etch silicon wafer directly using reactive ion etching(RIE) to form AWG layout, where space of waveguide 22.8μm in order

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to get sidecladding with 15μm thickness using thermal oxidation and leave core with 6μm width, the gap between two waveguides and the depth are not less than 36μm and 30μm, respectively, furthermore, these values should be optimized. Following that the silicon wafer is oxidized for thirty days under the hydrosphere atmosphere at 1050℃. The obtained SiO_2 layer thickness is about 15μm, which is used as undercladding and sidecladding, and a silicon layer is left at the side of waveguide, here we name it as side-silicon layer. The third step is to deposit two successive glass particle layers using flame hydrolysis deposition (FHD) or PECVD which form the core with 6μm thickness and overcladding with 15μm thickness. Finally, the substrate with these two porous glass layers is heated to about 1000℃ for consolidation or annealing. Using this new method, side-silicon layer with higher thermal expansive coefficient can be remained between two waveguides, which the width and depth are marked w and d in Fig. 1, respectively.

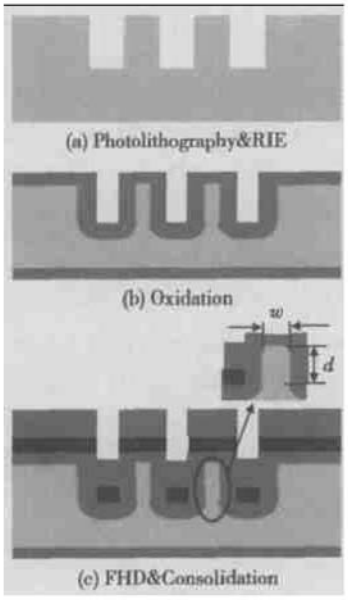

Fig. 1　Fabrication process of silica on silicon AWG

3　Calculation results and discussion

Figure 2 shows calculated stress distribution of one waveguide of AWG in parallel and perpendicular to the wafer surface using FEM[5]. The

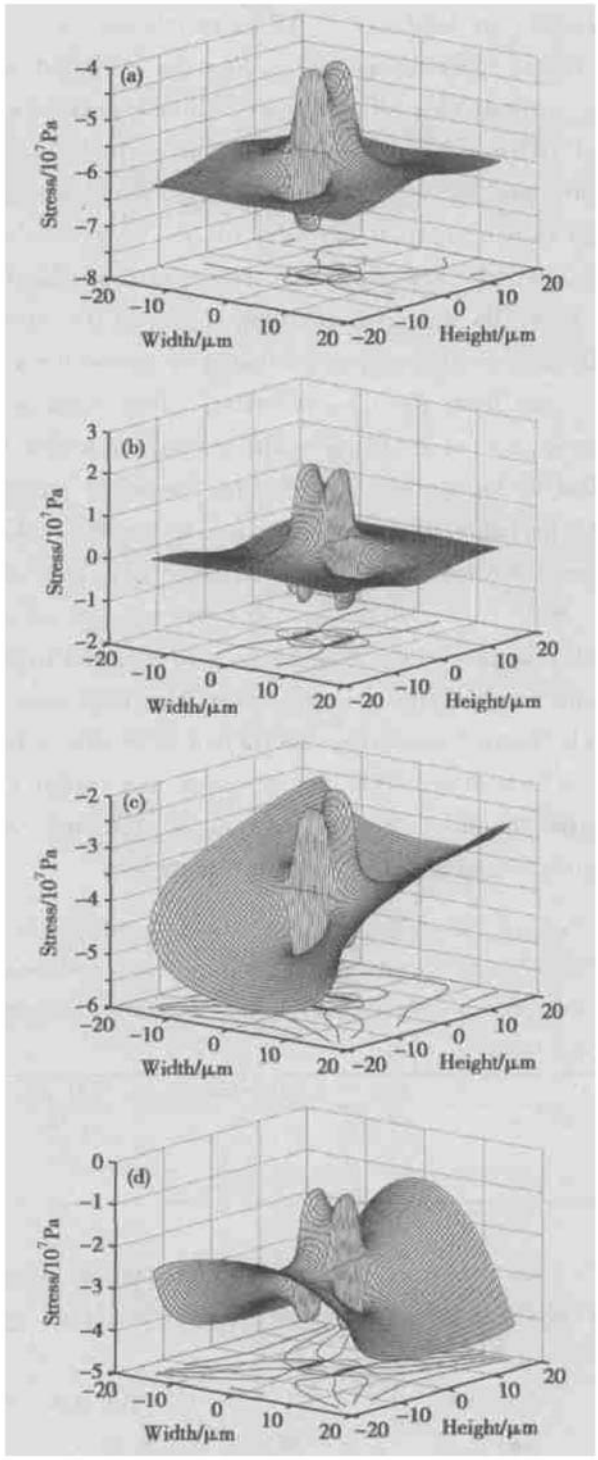

Fig. 2　Stress distribution in parallel and perpendicular to the wafer surface　(a) Parallel to the wafer surface with w = 0; (b) Perpendicular to the wafer surface with w = 0; (c) Parallel to the wafer surface with w = 10μm, d = 36μm; (d) Perpendicular to the wafer surface with w = 10μm, d = 36μm

thermal expansion coefficient, Poisson's ratio, and Young's modulus used in FEM are specified for all

elements in Table 1[6,7]. All materials are assumed to be mechanically isotropic. Figures 2(a) and (b) are without side-silicon layer, while Figures 2(c) and (d) are with side-silicon layer with the width 10μm and depth 36μm, respectively. When without side-silicon layer, in parallel to the wafer surface one finds the expected compressive stress is resulted from the higher thermal expansion of the silicon substrate, while in perpendicular to the wafer surface one finds the core is suffered from expansive stress and the cladding is almost not so, which results in higher stress difference between parallel and perpendicular to the wafer. But compared to Figs. 2(a) and (b), Figures 2(c) and (d) show that not only in parallel, but also perpendicular to the wafer surface, the waveguide is also suffered significant compressive stress due to the existence of high thermal expansive coefficient side-silicon layer, which means that the stresses in parallel and perpendicular to the wafer can be matched each other, resulting in very low birefringence.

Table 1 Mechanical data used in the strain calculations: Young's modulus (E), Poisson's ratio (ν), and thermal expansion coefficient (α) for Si, SiO_2 cladding and core

	Si	SiO_2 cladding	SiO_2 core
$E/10^9$Pa	131	65	70
ν	0.28	0.17	0.2
$\alpha/10^{-6}K^{-1}$	3.6	0.5	1.2

Based on above calculated stress distribution, the changes in refractive index for triaxial stresses are

$$\Delta n_x = n_x - n = -B_2\sigma_x - B_1(\sigma_y + \sigma_z) \quad (1)$$

$$\Delta n_y = n_y - n = -B_2\sigma_y - B_1(\sigma_x + \sigma_z) \quad (2)$$

where the stress optical coefficients are $B_1 = 4.2\times10^{-12}$Pa and $B_2 = 6.5\times10^{-13}$Pa[8]. Refractive index $n = 1.444$, refractive index difference between core and cladding is 0.75%. The propagation constant is calculated based on the refractive index output from stress analysis by full-vector alternating direction implicit (ADI) iterative method[9]. Then birefringence index B is deduced: $B = (\beta_{TM} - \beta_{TE})/k_0$.

Birefringence index for different w and d of side-silicon layer is shown in Fig. 3. The results indicate that the waveguide birefringence depends on w and d. For given w, the birefringence index decreases sharper at $d < 36\mu$m than at $d > 36\mu$m. For given d, more width side-silicon layer helps to reduce the birefringence. The result means that by optimizing w and d, birefringence index can be lowered to 1.0×10^{-4}.

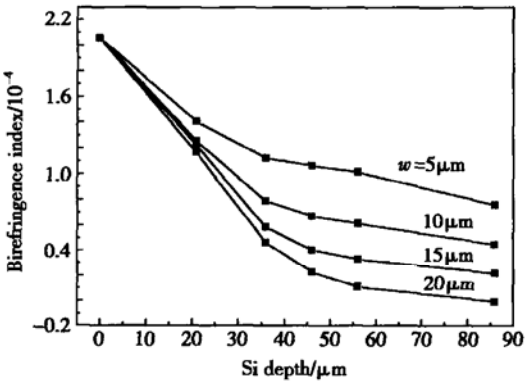

Fig. 3 Calculated birefringence as a function of w and d

Based on above analysis, low PDλ silica AWG is designed[10]. Considered the size of AWG device and difficulty in deep etching, w and d are specified as 10μm and 36μm, respectively, so the gap between two waveguides is 46μm. The correspondent parameters for 16 channels AWG are given in Table 2. The total area is 6cm×4.5cm, the output spectra simulated using single transmission function near center wavelength 1.5525μm for TE and TM mode is shown in Fig. 4. The result indicates that PDλ is about 0.07nm, which meets the demand of low PDλ AWG.

Table 2 Parameters for designed 16 channels AWG

n_s	n_c	n_g	m	R/μm	$\Delta L/\mu$m	Na
1.452397	1.450156(TE) 1.450235(TM)	1.456263	120	24105.104	128.469	100

n_s, n_c, n_g, m, R, ΔL, and Na are effective refractive index of slab waveguide, effective refractive index of channel waveguide, group index for n_c, diffraction order, focal length of slab waveguide, length difference of adjacent arrayed waveguide, and number of arrayed waveguides, respectively.

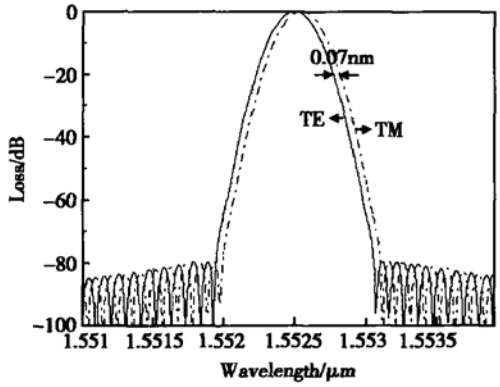

Fig. 4　Output spectra at λ_0 for designed AWG

4 Conclusion

We have presented a novel technology for fabricating buried silica AWG based on deep etching and thermal oxidation, which a silicon layer between waveguides is remained. Numerical analysis indicates that stresses of this kind of waveguide in parallel and perpendicular to wafer direction can be matched and low birefringence can be obtained by optimizing width and depth of side-silicon layer. Using this process, PDλ of designed AWG with 16 channels is only 0.07nm.

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偏振不灵敏硅基二氧化硅阵列波导光栅设计*

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摘要: 以深刻蚀和热氧化工艺为基础，提出了一种新的阵列波导光栅(AWG)制备技术. 这一工艺可使AWG中的波导侧向留有一硅层. 采用有限元法和有限差分束传播法分别计算了存在这一硅层时的波导应力分布和有效折射率. 结果表明由于这一侧向硅层的存在，使AWG中波导在水平和垂直方向的应力趋于一致，AWG的偏振相关波长明显减小.

关键词: 硅基二氧化硅；阵列波导光栅；应力；双折射；偏振相关波长；数值分析
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