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Design of Low-Voltage Low Noise Amplifiers with High Linearity*

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Abstract: A CMOS radio frequency low noise amplifier with high linearity and low operation voltage of less than 1.0V is presented. In this circuit, an auxiliary MOSFET in the triode region is used to boost the linearity. Simulation shows that this method can boost the input-referred 3rd-order intercept point with much less power dissipation than that of traditional power/linearity tradeoff solution which pays at least 1dB power for 1dB linearity improvement. It is also shown that the size of the common-gate PMOS transistor needs to be optimized to reduce its loaded input impedance so as not to degrade the linearity due to high voltage gain at its source terminal. The simulation is carried out with TSMC 0.18μm RF CMOS technology and SpectreRF.

Key words: low-voltage; radio frequency; CMOS; low noise amplifier; linearity
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1 Introduction

With the scaling-down of CMOS process, the radio frequency (RF) system on a chip becomes economically inevitable. Much attention has been paid to low voltage design[1]. The low noise amplifier (LNA) must have high dynamic range[2], defined by its noise floor and the 3rd-order intercept point (IP_3), which means tradeoff in gain, noise, linearity, and power dissipation[3,4].

To boost IP_3, feedforward[5,6] can be used, but at the cost of power hungry auxiliary unit. Volterra series analysis of bipolar transistor (BJT) amplifiers has led to in-band and out-of-band termination in discrete BJT amplifiers[7~9]. However, it is burdensome in CMOS design. Compensation using MOSFETs with different gate bias has been reported[10], but the DC isolation problem and the broadband feature make it unsuitable for integrated tuning LNAs. Compensation using triode transistor[11] is free of these problems and more than 10dB improvement has been achieved by differential cascode LNA with 2.5V supply[12], while it has not been demonstrated in folded cascode LNAs operated at lower supply voltage.

In this paper, the analysis on the nonlinearity in MOSFET and the operation of triode MOSFET boosting IP_3 are given. Simulation results of folded cascode LNAs and the discussion on the results and design guidelines are presented.

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2　CMOS LNA and IP3-boost

Shown in Fig. 1(a) is a popular low-voltage folded cascode LNA. The drain current of M1 in the saturation region can be written as

$$I_{ds} = \beta_0 \frac{1}{(1 + \theta_1 V_{od})(1 + \theta_3 V_{od})} \times V_{od}^2 \quad (1)$$

where β_0, θ_1, and θ_3 are all device parameters[13, 14], and V_{od} is the overdrive voltage. If the noise in M2 is neglected, the noise factor of the LNA is[15]

$$F = 1 + \frac{1^2}{Q_s} \times \frac{\gamma}{\alpha} \times \frac{\omega}{\omega_T} + \frac{Q_s^2 + 1^2}{Q_s} \times \frac{\delta\alpha}{5p^2} \times \frac{\omega}{\omega_T} + \frac{2}{p} \times |c| \sqrt{\frac{\delta\gamma}{5}} \times \frac{1^2}{Q_s} \times \frac{\omega}{\omega_T} \quad (2)$$

and the power gain

$$G_m \propto g_m Q_s \quad (3)$$

where g_m is the transconductance of M1, Q_s stands for the ratio of the gate-source RF voltage to that of input source; γ, α, δ, c, p, and ω_T are all device- and/or bias-dependent parameters. Though large Q_s is beneficial for high gain and low noise, it degrades the linearity. Large V_{od} is desirable for high linearity, but the power efficiency suffers. Usually, V_{od} is in the range of 100~ 200mV and Q_s is 2~ 5 for the sake of noise and gain. Unfortunately, the linearity is poor in this case.

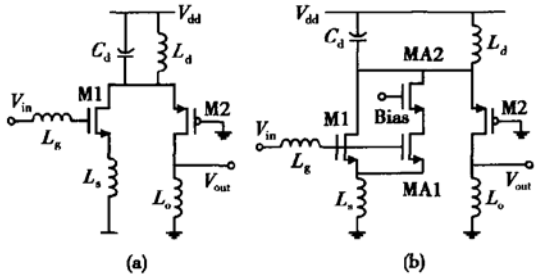

Fig. 1　Schematic of folded degeneration LNA　(a) Typical configuration; (b) Modified configuration

The small signal drain current with weakly nonlinear can be expanded in Taylor series as

$$i_{ds} = g_1 v_{gs} + \frac{1}{2} g_2 v_{gs}^2 + \frac{1}{6} g_3 v_{gs}^3 + \cdots \quad (4)$$

where v_{gs} is the small signal gate-source voltage.

Usually, it can be assumed that g_1 is identical to g_m, and g_2, g_3, …, are the successive derivatives of drain current over gate-source voltage, respectively. IP3 is determined by g_1/g_3, which the larger is, the larger IP3. Simulation is used to find g_1, g_2, and g_3 in all operating regions of the MOSFET. It is shown that, g_1(Fig. 2(b)) of M1 increases with gate voltage and then saturates. On the curve of g_3 (Fig. 2(d)), there are two humps (positive and negative) in the vicinity of V_{th}(0.5~ 0.6V). The usual operating point is located near and right to the negative hump, where g_1/g_3 and IP3 are small.

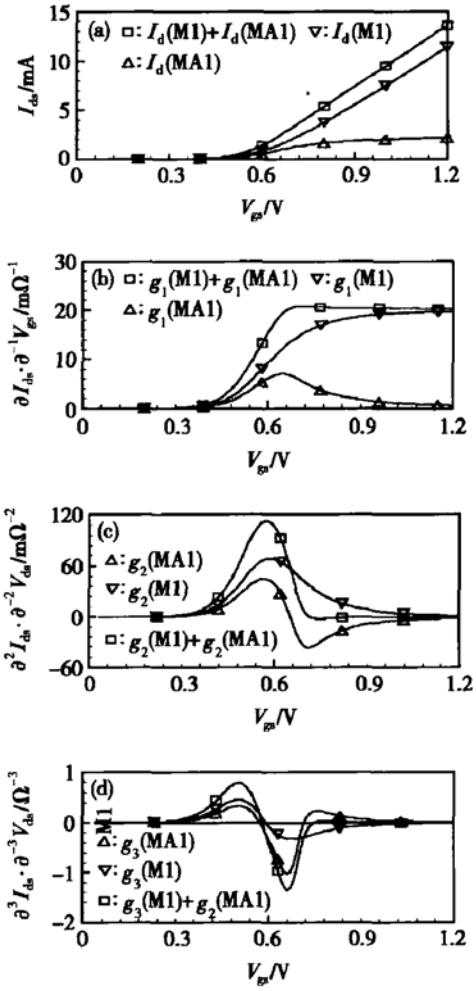

Fig. 2　DC I-V characteristics and its derivatives of M1, MA1, and M1 plus MA1

g_1/g_3 can be enhanced by using auxiliary MOSFETs to eliminate the negative hump while g_1 changes little as shown in Fig. 1(b). Here, M1 is the main amplification branch; MA1 in the auxil-

iary branch is in the triode region while MA2 is saturated. When the drain and gate voltage of MA2 is fixed, with the increase of MA1 gate voltage, the drain voltage of MA1 drops and the current of the auxiliary branch increases quickly, until at a point, the drain-source voltage of MA1 approaches zero and it saturates (Fig. 2(a)). As well as the sizes, the gate bias of MA1, the gate and the drain voltage of MA2 can be freely chosen to make the composite g_3 (of the auxiliary and the main branch) almost zero over a wide range. To avoid using coupling capacitor, the gate of MA1 is connected to that of M1 and the drain of MA2 to that of M1. For simplicity, the sizes of MA1 and MA2 are the same as that of M1 while the gate voltage of MA2 is adjusted to minimize the absolute value of the composite g_3.

3 Simulation results

Six LNAs with commercially available TSMC 0.18μm RF CMOS technology were simulated with SpectreRF. Among them, three were with M2 of shorter length (0.24μm): ST (short M2 and typical topology) and SD (short M2 and with double-sized-M1) were typical LNAs, SA (short M2 and with auxiliary MA1) had an auxiliary branch. SD had a double-width M1 compared with the other two. Analogously, three LNAs with M2 of longer channel length (0.36μm) were LA (long M2 and with auxiliary MA1), LT (long M2 and typical topology), and LD (long M2 and with double-sized M1).

The degenerating inductor, the load inductor and the one connected at the drain of M1 were implemented on-chip based on the model provided and validated by TSMC.

S-parameter analysis around 2.4GHz was carried out, tuning the input and output matching, measuring the noise figure and small-signal gain. Periodic steady state (PSS) analysis shows that the -1dB gain compression points (P_{-1dB}) of these circuits were around -15~ -20dBm. To find IP_3, two-tone tests were performed with input RF power step of 5dBm from -50dBm to 0dBm and -35dBm, 15~ 20dB less than P_{-1dB}, was chosen as the extrapolation points.

The voltages and voltage gains were found by PSS analysis. The voltage gains at the drain of M1 were measured at the input RF power level in the vicinity of -35dBm. The simulation results are summarized in Table 1 and Table 2.

Table 1 Summary of the simulation results of the LNAs with short channel PMOS

Parameters	ST	SA	SD
G_P/dB	15.7	15.3	16.6
$A_{v,D1}$	1.17	1.46	2.0
NF/dB	1.6	1.4	1.2
P_{-1dB}/dBm	-19.1	-18.4	-19.5
IIP_3/dBm	-3.8	-1.15	-2.95
OIP_3/dBm	11.9	14.25	13.65
$I_{D,M1}$/mA	2.87	2.87	5.73
$I_{D,M2}$/mA	9.55	9.43	9.30
$I_{D,MA1}$/mA	—	1.46	—
$I_{D,total}$/mA	12.42	13.76	15.04
V_{dd}/V	1.2	1.2	1.2
L_{M1}/μm	0.18	0.18	0.18
L_{M2}/μm	0.24	0.24	0.24

Table 2 Summary of the simulation results of the LNAs with long channel PMOS

Parameters	LT	LA	LD
G_P/dB	15.0	13.9	16.3
$A_{v,D1}$	0.8	0.96	1.39
NF/dB	1.5	1.5	1.2
P_{-1dB}/dBm	-19.0	-16.7	-16.7
IIP_3/dBm	-4.85	3.4	-0.6
OIP_3/dBm	10.15	17.3	15.5
$I_{D,M1}$/mA	2.88	2.88	5.76
$I_{D,M2}$/mA	12.2	12.17	12.09
$I_{D,MA1}$/mA	—	1.46	—
$I_{D,total}$/mA	15.08	16.5	17.85
V_{dd}/V	1.2	1.2	1.2
L_{M1}/μm	0.18	0.18	0.18
L_{M2}/μm	0.36	0.36	0.36

4 Analysis

Simulation shows that the addition of auxiliary branch improved IIP_3 and OIP_3 (the input- and output-referred intercept point). Table 1 shows that in the shorter M2 case (ST versus SA), IP_3 were im-

proved more than 2dB, while Table 2 shows that in the longer M2 case (LT versus LA), IP_3 were boosted by 7~ 8dB.

P_{-1dB} were improved only tenths of dB in the case with shorter channel M2 and no more than 3dB in the case with longer channel M2. It is expected from the physical insight. Since the compensation itself cannot eliminate nonlinearity, with the increase of input RF power, the power of the nonlinear product increases faster than the fundamental product. With the power drawn from the supply fixed, the gain is compressed.

The enhancement of P_{-1dB} is mainly due to the drops of Q_s. Also, improvement of IP_3 partially comes out of it. This is confirmed by comparing SD versus ST and LD versus LT. Doubling M1 size halves Q_s, so both SD and LD show larger P_{-1dB} and IP_3, yet less than those of SA and LA. The compensated LNAs exhibit higher IP_3 and P_{-1dB} while dissipate less DC power.

The impact of voltage gain at M1 drain, $A_{v,D1}$, is notable. It is seen that circuits with longer channel M2 show higher linearity and smaller voltage gain at the drain terminal of M1 as well, than their counterparts with shorter channel M2, respectively. The explanation follows below.

It is a key feature of cascode LNA that the voltage gain at the drain of M1 is small so that feedback through the gate-drain capacitor is negligible. The analysis in Part 2 is based on this unilateralism; otherwise, high swing voltage at the drain terminal of M1 complicates the nonlinear behavior of MOSFET through the Miller effect and the channel length modulation effect as well. As the voltage swing at source of M2 gets higher, the nonlinearity of M2 begins manifesting itself though the overdrive of M2 may be high. Furthermore, the supply and thus the overdrive voltage may be low and thus the nonlinearity of M2 may not be negligible if the voltage swing is high. This analysis also applies to the circuit in Fig. 1(b).

One way to reduce the channel length modulation effect is to increase the length of M1, but this will decrease the cut-off frequency and the Miller effect remains. So, it is necessary to reduce the impedance seen from the drain of M1 and the voltage gain at the drain of M1. In the folded topology, the drain load of M1 is a parallel LC-tank tuned at the working frequency. Thus, the input impedance of M2 must be reduced.

For the first-order proximity, the input impedance of the common-gate MOSFET is equal to $1/g_m$, whatever its drain load is. For short channel devices, however, this is invalid. For 0.18μm process, $g_m r_{ds}$ of the MOSFET is usually in the order of tens. Simple calculation indicates that the real part of the input impedance of common-gate MOSFET is

$$\mathrm{Re}(Z_{in}) = \frac{r_{ds} + Z_L}{g_m r_{ds}} \tag{5}$$

where r_{ds} is the drain output resistance, and Z_L is the load impedance and assumed to be real. Thus for the circuits of Fig. 1(a), the voltage gain at the drain terminal of M1 is

$$A_{v,D1} = \frac{v_{d,gnd}}{v_{gs}} \cong \frac{g_{m,1}(r_{ds,2} + Z_L)}{g_{m,2} r_{ds,2}} \tag{6}$$

If $r_{ds,2}$ is dominant in the second term of the numerator in Eq. (6), simply increasing $g_{m,2}$ can reduce the voltage gain. Unfortunately, the above condition is usually not true and Z_L is dominant or comparable with $r_{ds,2}$ as the load of M2 is an inductor. Note that for fixed channel length and gate overdrive, $g_m r_{ds}$ is almost constant; it is almost impossible to reduce $A_{v,D1}$ by simply adjusting the W/L ratio of M2.

Increasing $g_{m,2}$ can reduce the voltage gain at the cost of large bias current. However, this means larger DC power. This situation leads to using M2 with longer channel, which has larger r_{ds}. The simulation indicates that the voltage gain at M1 drain terminal is reduced and the linearity is improved.

The channel length of M2 can not be too large for the sake of its cut-off frequency. The low supply voltage limits the gate overdrive and demands that channel length should be short enough. Second, the parasitic capacitance of M2 should be

small enough. Lastly, to avoid loss incurred by the LC-tank, the condition[16] of Eq. (7) should be satisfied,

$$g_{m,2} > \omega_0 C_d / Q_L \quad (7)$$

where C_d is the tank capacitor, including those parasitic, and Q_L is the quality factor of the LC-tank.

Shown in Fig. 3 are the simulation results of IIP_3 versus DC power. The dash lines indicate the ~ 1dB/dB relationship between the DC power and IIP_3. In Fig. 3(a), only the power of MA1 and M1 of each LNA is taken into account, while in Fig. 3 (b), the total power of each LNA is taken into account. It can be concluded that the folded LNA with auxiliary branch and reasonably longer channel M2 balances DC power and IIP_3 excellently. Its power expense is much less than those of simple amplifiers without any compensation, i. e., double power dissipation for 3dB dynamic range improvement[4]. Moreover, this circuit works well with low supply voltage even less than 1.0V and total power dissipation will decrease as the power supply voltage decreases.

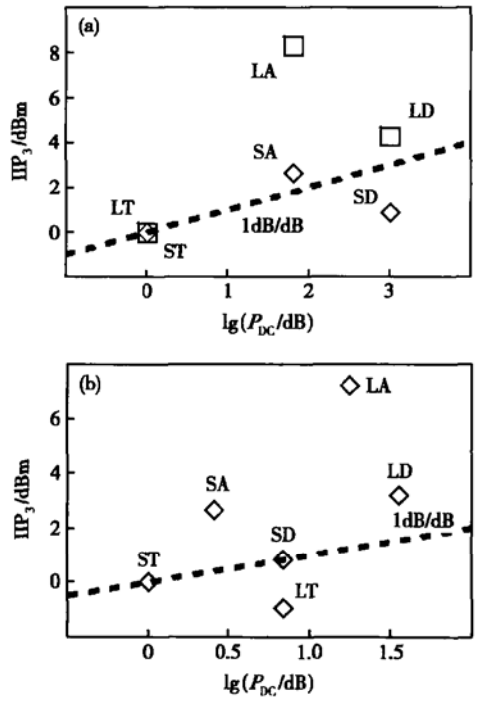

Fig. 3 IIP_3 versus DC power of different LNAs (normalized to that of ST)

5 Conclusion

In this paper, a CMOS RF LNA with high linearity and low voltage is presented. Simulation shows that the auxiliary branch in the folded LNA can boost IP3 with much less power dissipation than 1dB power increase for 1dB linearity improvement. Design tradeoffs are analyzed and design guidelines are also given.

References

[1] Li Tianwang, Zeng Xiaojun, Hong Zhiliang. Design of 1 V 2.5GHz voltage controlled oscillator. Chinese Journal of Semiconductors, 2003, 24(1): 80(in Chinese) [李天望, 曾晓军, 洪志良. 1V 2.5GHz 压控振荡器设计. 半导体学报, 2003, 24(1): 80]

[2] Aparin V, Larson L E. Analysis and reduction of cross-modulation distortion in CDMA receivers. IEEE Trans Microw Theory Tech, 2003, 51(5): 1591

[3] Razavi B. CMOS technology characterization for analog and RF design. IEEE J Solid-State Circuits, 1999, 34(3): 268

[4] Abidi A A, Pottie G J, Kaiser W J. Power-conscious design of wireless circuits and systems. Proc IEEE, 2000, 88(10): 1528

[5] Lin M, Li Y, Chen H. A novel IP3 boosting technique using feedforward distortion cancellation method for 5GHz CMOS LNA. IEEE Radio Frequency Integrated Circuits Symposium, 2003: 699

[6] Ding Y, Harjani R Y. A + 18dBm IIP3 LNA in 0.35μm CMOS. Digest of Technical Papers of IEEE International Solid-State Circuits Conference, 2001, 443: 162

[7] Fong K L, Meyer R G. High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages. IEEE J Solid-State Circuits, 1998, 33(4): 548

[8] Fong K L. High-frequency analysis of linearity improvement technique of common-emitter transconductance stage using a low-frequency-trap network. IEEE J Solid-State Circuits, 2000, 35(8): 1249

[9] Aparin V, Persico C. Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits. Digest of International Microwave Symposium, 1999, 3: 977

[10] Kim T W, Kim B, Lee K. Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors. IEEE J Solid-State Circuits, 2004, 39(1): 223

[11] Tanaka S, Behbahani F, Abidi A A. A linearization technique for CMOS RF power amplifiers. Digest of Technical Papers of Symposium on VLSI Circuits, 1997: 93

[12] Youn Y S, Chang J H, Koh K J, et al. A 2GHz 16dBm IIP3 low noise amplifier in 0.25μm CMOS technology. Digest of Technical Papers of IEEE International Solid-State Circuits Conference, 2003, 1: 452

[13] Klaassen D B M. MOS MODEL 9 from physics to equations. Proceedings of the MOS MODEL 9 Workshop, 1996

[14] Lee T H. The design of CMOS radio-frequency integrated circuits. Cambridge: Cambridge University Press, 1998: 73

[15] Cao K, Yang H, Wang H. The design of CMOS RF low noise amplifiers. Proceedings of 5th IEEE International Conference on ASIC, 2003: 1106

[16] Abou-Allam E, Nisbet J J, Maliepaard M C. A low-voltage 1.9-GHz front-end receiver in 0.5-μm CMOS technology. IEEE J Solid-State Circuits, 2001, 36(10): 1434

高线性低电压低噪声放大器的设计*

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摘要: 研究了一种具有高线性的CMOS低噪声放大器，其工作电压可以低于1V. 在这个电路中，加一个工作在线性区的辅助MOS管以提高线性特性. 仿真表明这种方法可以提高输入三阶交截点，其代价远小于传统方法为获得1dB线性度改善而必须增加1dB功耗的代价. 为了降低该电路中的共栅PMOS管的有载输入阻抗，不使其源极处的电压增益过大而降低电路的线性特性，必须优化其尺寸. 仿真使用的模型是TSMC 0.18μm射频CMOS工艺库，仿真工具是Cadence的SpectreRF.

关键词: 低电压；射频；CMOS；低噪声放大器；线性特性

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