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Study on Synchro-Epitaxy of Poly- and Single Crystal Silicon

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Abstract: Synchro-epitaxy is introduced and a "two periods epitaxy" process is proposed. The influence of the flows of SiH_4 N_1, N_2, deposition time t_1, t_2, and epitaxial temperature T on epilayer quality (embodied by α) is reported. The shorter initial inducing time t_1 and larger flows of SiH_4 are, the wider single crystal strips are. But the quality of epilayer may be poor. The optimum conditions are: N_1= 13.1~ 17.5sccm, N_2= 7.0~ 7.88sccm, and t_1= 30~ 50s. The influence of temperature is complex: when T is lower than 980℃, single crystal strips increase with T; when T is higher than 980℃, single crystal strips decrease with T. It reaches maximum near 980℃.

Key words: synchro-epitaxy; nucleation; CVD
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1 Introduction

As one of the basic processes for semiconductor manufacturing, silicon deposition has attracted great attention all the time. In recent years, the researches are focused on the fabrication of SOI[1,2], strained Si/SiGe HBT material[3,4], poly-silicon[5,6] on different substrates by various ways. These works involve crystal silicon epitaxy, poly-silicon epitaxy or selective epitaxy[7,8]. However synchro-epitaxy is seldom mentioned.

Synchro-epitaxy is the process that the poly-silicon layer (deposited on SiO_2) and the single crystal layer (deposited on crystal silicon) are synchro-grown by low reaction temperature chemical vapor deposition (CVD) using silane (SiH_4). For this kind of epitaxy, the width and depth of the single crystal layer is decisive to the device's performance. They will determine the device's current, source-gate breakdown voltage and transconductance etc. In addition, the connected quality of single crystal layer with the poly-silicon layer is also essential. It plays the same role for the device. That's the sticking point for the synchro-epitaxy.

2 Process control and the epitaxial quality parameter α

A horizontal double-decker water-cooling quartz tube has been used as a reactor. The carrier gas is H_2. The source temperature is fixed at 21℃, the pressure at 9.43×10^4Pa.

Before epitaxy, a silicon dioxide grid was formed on the substrate. Its width and space (the initial width of the single crystal strip) are 4.7~ 4.9μm and 2.1~ 2.3μm, respectively; its thickness is about 1.2μm (see Fig. 1).

To ensure poly-silicon layer and single crystal layer be synchro-grown, two periods epitaxy is introduced. It includes the initial inducing period and regular growth period.

During the initial inducing period, the flow rate of the silane (marked as N_1) is higher. This

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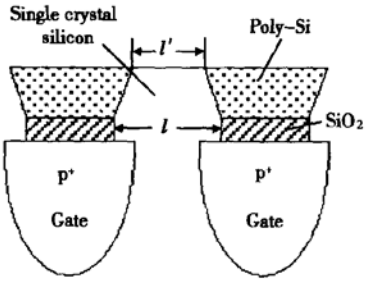

Fig. 1 Dielectric covered gates structure

may lead to better nucleation and growth on the oxide. When the poly-silicon nuclei on SiO_2 are saturated and permeated, the flow rate of the silane is reduced to regular value (marked as N_2). The epitaxy enters into the second stage growth.

Figure 2 gives the SEMs of the epilayer with vertical incident light (a) and with inclined incident light (b). These show that stripes on the SiO_2 are poly-silicon layer and those between the SiO_2 are single crystal.

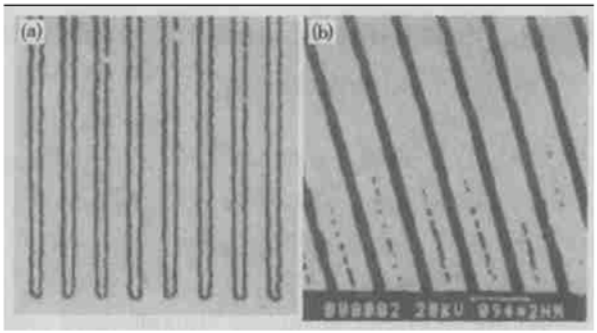

Fig. 2 SEM of the poly silicon and single crystal stripes grown by the synchro-epitaxy (a) SEM with vertical incident light, wide stripes are poly-silicon, narrow single crystal; (b) SEM with inclined incident light, dark stripes are poly-silicon, light single cyrstal

To feature the quality of epitaxy quantificationally, a parameter α is introduced. It is defined as:

$$\alpha \equiv \frac{l'}{l} \qquad (1)$$

where l' is the final width of single crystal silicon strip after epitaxy, and l is the initial width (see Fig. 1) before epitaxy.

3 Experiment results and analysis

For different options of process, the epitaxial results vary greatly. There are three kinds of typical results:

(1) $\alpha > 1$, the finial width of the single crystal strip is larger than initial value and is ill connected with poly-silicon layer. In some extension, single crystal silicon is deposited along the side of SiO_2. In this case, the source-gate breakdown voltage is low.

(2) $\alpha \ll 1$, transversal straggling of poly-silicon is so serious and the width of the single crystal strip is so narrow that the current feature of the device is poor. It's unfavorable for the materialization of designed purpose.

(3) α is about 0.6~0.9, the single crystal layer is well connected with the poly-silicon layer and the poly-silicon is compactly deposited on the top of and the side of SiO_2. Meanwhile, the crystal strip is wide enough and the property of the device is optimum.

There are many process parameters that will influence α. They are: initial inducing time t_1, silane flow rates (N_1 and N_2), the thickness of epitaxial layer (determined by N_2 and regular growth time t_2), epitaxial temperature T etc. They will be discussed separately.

3.1 Influence of initial inducing time t_1 on α

When the epitaxial temperature T, the flow rates of silane N_1, N_2, and the regular growth time t_2 are determined, the relationship of α and initial inducing time t_1 is figured in Fig. 3. It shows that:

(1) If t_1 is less than 25s, then α is larger than 1. Meanwhile, the poly-silicon layer is imperfect and some big grains of poly-silicon are formed. The single crystal stripes are formed along the side of SiO_2 and sometimes are separated from the poly-silicon. The joints of the crystal strips and poly-silicon strips are bad. This may result in large leaky current and low breakdown voltage of device.

(2) When 30s ≤ t_1 ≤ 60s, α is in the range of 0.6~ 0.9, the poly-silicon is compactly deposited on the top and the side of SiO_2. Meanwhile poly-silicon strip is properly marching with the crystal strip. This is just what we want.

(3) If t_1 is longer than 60s, the single crystal strip is also well connected with the poly-silicon strip, but its width decreases greatly. The current will be low and can't fit the demand of high power device. On all accounts, the initial inducing time should be limited in the range of 30~ 50s for the given condition.

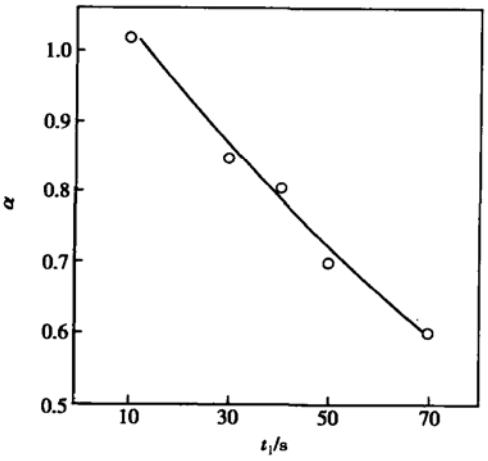

Fig. 3　Relationship between α and t_1

3.2 Influence of the silane flow rate on α

When epitaxial temperature T and initial inducing time t_1 are determined, the relationship of silane flow rate (N_1 and N_2) and α is shown in Fig. 4. In addition, to keep the thickness of epitaxial layer approximately the same, t_2 changes with N_2. If the initial inducing time t_1 and initial inducing flow rate N_1 are suitable, α will be less than 1 and the interface of poly-silicon strip and single crystal strip integrates well. Under this precondition, the more silane flow rates (both N_1 and N_2) are, the less α will be. To make the poly-silicon nucleated easily and saturated quickly and ensure the poly-silicon layer and the single crystal layer synchro-grown, it is necessary for the high silane flow rate during initial inducing period. And to get large α, the silane flow rate should be dropped during regular growth period. The optimum flow rates are: N_1 = 13.1~ 17.5sccm, N_2 = 7.0~ 7.88sccm.

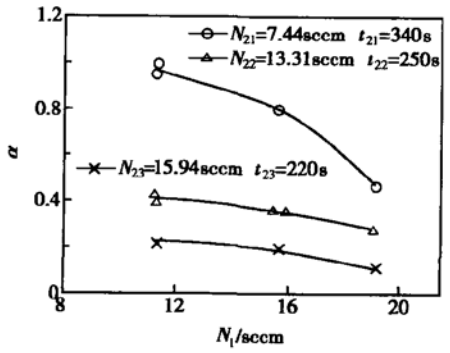

Fig. 4　Relationship between α and the flux of SiH_4

3.3 Influence of regular growth time t_2 on α

Fixing t_1, N_1, N_2, and T, the influence of regular growth time on α is shown in Fig. 5. It is very clear that there exits a flexed point of the curve, and the curve is divided into three parts:

(1) If t_2 is less than 5min, α is larger and tends to 1 as t_2 tends to 0. During this period, α changes gently with t_2—increasing t_2 from 3min to 5min, α changes from 0.94 to 0.8, the variation velocity is 0.07/min.

(2) Thereafter, α decreases sharply with t_2—increasing t_2 from 5min to 6min, α decreases from 0.8 to 0.38, and the reduction is 0.32 within 1min.

(3) From here on, α falls slowly again—increasing t_2 from 6min to 10min, the decreases of α is only 0.08 (from 0.38 to 0.30), the reducing velocity is 0.02/min.

At the beginning of regular growth, the ledge of SiO_2 whose surface is deposited by poly-silicon provides conglutination atoms that accelerate silicon deposit ion on single crystal. So the deposition rate on single crystal is faster than that on poly-silicon and transversal growth of poly-silicon is slow. As the deposition goes on, the sidestep height of SiO_2 is reduced (see Fig. 6). When the height drops low enough, the depositing rate of single crystal slows down but the poly-silicon depositing rate

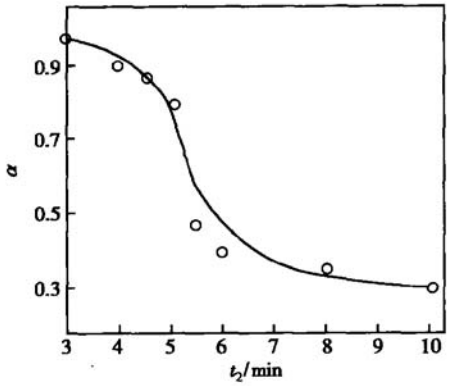

Fig. 5 Relationship between α and t_2

near the corner speeds up, and α reduces sharply. When the step fills up, the transversal extending tends to stop, the width of single crystal strip fixed.

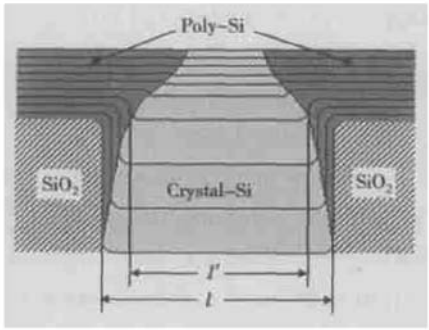

Fig. 6 Sketch of poly-Si transversal straggling

3.4 Influence of epitaxial temperature on α

The temperature is an important parameter for CVD. The relationship of T and α is shown in Fig. 7. When T is lower than 980℃, α increases with T and reaches maximum near 980℃. And then α decreases as T goes up. This variation lies in different control mechanism of deposition speed. For the benefit of wider single crystal strip, the optimum temperature should be controlled within 980 ±5℃.

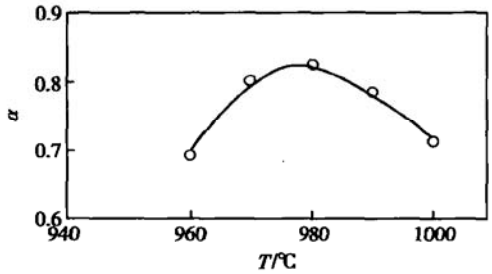

Fig. 7 Relationship between α and T

4 Conclusion

Synchro-epitaxy is a complicated technics. There are many factors that will influence the quality of epitaxial layer, such as flow rate of SiH_4 (including N_1 and N_2), growth time of each period, epitaxial temperature and so on. All these factors are correlative with each other. The optimum epitaxial result can only be obtained by adjusting all the parameters synthetically. As for our device structure, the optimum epitaxial conditions are:

(1) Flow rate of SiH_4: N_1= 13.1~ 17.5sccm, N_2= 7.0~ 7.88sccm;

(2) Growth time: t_1= 30~ 50s, $t_2 \leqslant 300$s;

(3) Epitaxial temperature: T= 980±5℃.

The performances of the device fabricated by using these process parameters are discussed in another paper[9].

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多晶硅、单晶硅同步外延研究

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摘要: 介绍了多晶硅、单晶硅的同步外延. 采用两步外延工艺, 研究了硅烷流量、外延时间以及外延温度对外延质量参数 α 的影响. 硅烷流量大、初始诱生时间短, 则单晶硅条宽, 多晶硅横向蔓延弱, 但外延层质量可能较差. 较优的条件是: 硅烷诱生生长流量为 13.1~ 17.5sccm, 正常生长流量为 7.0~ 7.88sccm, 初始诱生时间为 30~ 50s. 温度影响较复杂, 当温度低于 980℃时, 单晶硅条宽随温度增加而增加, 在 980℃附近达到最大, 随后随温度增加单晶条宽降低.

关键词: 同步外延; 成核; 化学气相淀积

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