

A DC-to-32GHz 2Bit MEMS Phase Shifter

Lou Jianzhong^{1,2}, Zhao Zhengping^{2,3}, Yang Ruixia², Lü Miao³ and Hu Xiaodong³

(1 College of Electronic and Information Engineering, Hebei University, Baoding 071002, China)

(2 College of Information, Hebei University Technology, Tianjin 300130, China)

(3 Micro/Nano Technology Centre, Hebei Semiconductor Research Institute, Shijiazhuang 050051, China)

Abstract: A two-bit phase shifter with distributed microelectromechanical system (MEMS) transmission line (DMTL) is developed, and a novel structure which be actuated by coplanar waveguide transmission line (CPW-actuation structure) is proposed, which can reduce the actuation voltage significantly. The measured result, with actuation voltage less than 20V, $0^\circ/20.1^\circ/41.9^\circ/68.2^\circ$ phase shift and -1.2 dB insert loss at 20GHz, is demonstrated, and insertion loss/return loss is better than -1.8 dB/ -11 dB from DC to 32GHz. The experimental results highlight the potential of a low-loss and broadband digital MEMS phase shifter on a high-permittivity substrate.

Key words: MEMS; phase shifter; CPW-actuation structure

EEACC: 2575: 1320: 1350

CLC number: TN4

Document code: A

Article ID: 0253-4177(2004)11-1386-05

1 Introduction

Microwave and millimeter-wave phase shifters are essential components in radar system, wireless, and satellite broadband communication network. Traditional phase shifters are generally built on GaAs substrate and use MESFET's, pHEMT's, or p-i-n diode as switch. But relative high insertion loss is the main drawback of the traditional phase shifters, and decreasing the loss can drastically reduce the cost and weight of wireless system. Fortunately, RF MEMS technology provides a possible solution for this. A lot of papers about MEMS phase shifter with the operating band up to 100GHz were published in last 5 years. The main types include switched line, reflect-line, and DMTL phase shifter. The DMTL phase shifter draws more and more attentions because of low insertion loss, low power dissipation, and broadband characteristic.

The DMTL phase shifter consists of a high impedance line that is loaded periodically with the MEMS bridges, which act as varactors. MEMS capacitance is varied by using an actuation voltage to vary the bridge height of the MEMS, thus changing distributed loading and further the impedance of transmission line. By changing transmission line impedances, phase velocity changes which results in a phase shift.

The DMTL phase shifter was first done in University of Michigan by Barker and Rebeiz^[1]. It was an analog phase shifter. A coplanar waveguide (CPW) transmission line fabricated on a $500\mu\text{m}$ quartz substrate with fixed-fixed beam MEMS bridge capacitors placed periodically over the transmission line. The phase shift is -2 dB loss/ 118° at 60GHz and -1.8 dB loss/ 84° at 40GHz. Borgioli et al.^[2] firstly presented 1bit digital DMTL phase shifter. The phase shifter consists of a 8.58mm-long coplanar waveguide transmission line on quartz substrate, loaded periodically with 11 shunt

Lou Jianzhong male, was born in 1966, PhD candidate. He is engaged in research on MEMS for RF applications.

Received 31 January 2004, revised manuscript received 13 May 2004

©2004 The Chinese Institute of Electronics

MEMS capacitors. The spacing between the MEMS capacitors is $780\mu\text{m}$. To reduce the down-state capacitance value, MEMS bridge and fixed MIM capacitor series configuration are adopted. In 75V bias voltages, the phase shift is 180° at 25GHz and 270° at 35GHz. The insertion loss is less than -1.17dB at 25GHz and -1.69dB at 35GHz. The return loss is better than -11dB over a DC-to-35GHz for up and down-state.

A 2bit DC-to-32GHz DMTL phase shifter was prepared on high-resistivity silicon substrate in this paper, and a novel CPW-actuation configuration is proposed for the first time to reduce the actuation voltage.

2 Design of MEMS phase shifter

The schematic structure and the lumped-element circuit model of the DMTL phase shifter are shown in Fig. 1. The operating frequency of DMTL phase shifter depends on the Bragg frequency. In

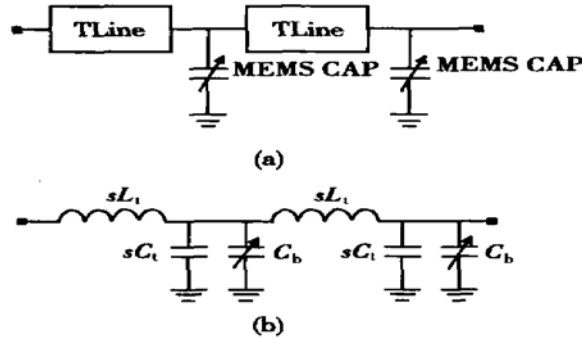


Fig. 1 DMTL phase shifter (a) Schematic structure; (b) Lumped-element circuit model

order to operate up to 30GHz, the Bragg frequency must be designed over 60GHz ^[3]. The Bragg frequency is decided by^[4]:

$$f_{\text{Bragg}} = \frac{1}{\pi s \sqrt{L_1 (C_1 + C_b/s)}} \quad (1)$$

where s is periodic spacing of the MEMS bridges, L_1 and C_1 are respectively the inductance and capacitance in per unit-length of the unloaded CPW line. They are given by

$$C_1 = \frac{\sqrt{\epsilon_{\text{eff}}}}{c Z_0} \quad \text{and} \quad L_1 = C_1 Z_0^2 \quad (2)$$

where ϵ_{eff} and Z_0 are the effective permittivity constant and impedance of unloaded CPW line, c is the free-space velocity.

Substituting formula (2) to (1), we obtain:

$$f_{\text{Bragg}} = \frac{1}{\pi s \sqrt{\epsilon_{\text{eff}}/c^2 + \sqrt{\epsilon_{\text{eff}} C_b Z_0/c s}}} \quad (3)$$

From formula (3), the periodic spacing and loaded capacitance should be reduced to make the Bragg frequency higher, and the characteristic impedance of DMTL must be close to 50Ω to reduce the return loss.

In our instance, the range of the characteristic impedances is chosen to be from 40 to 59Ω . Therefore, the impedance of unloaded CPW line is designed as 62Ω ($w = 30\mu\text{m}$, $\text{gap} = 40\mu\text{m}$). The periodic spacing is $500\mu\text{m}$. The maximal loaded capacitance is derived to be 145fF from formula (3).

The impedance of loaded CPW line is given by:

$$Z_l = \sqrt{\frac{L_1}{C_1 + C_b/s}} \quad (4)$$

The impedance of loaded CPW line is designed to be 40Ω ; from formula (4), the down-state capacitance of MEMS bridge is derived to be 80fF . A narrow center conductor of CPW transmission line is designed to get such a tiny down-state capacitance, which leads to very high actuation voltage. A CPW-actuation configuration is proposed to reduce the actuation voltage. The configuration is shown in Fig. 2(a). Actuation voltage was applied between the membrane and CPW transmission line. The actuation voltage decreases significantly since the actuation area is increased and the loaded capacitance decreases significantly. The actuation voltage is given by^[5]:

$$V_p = \sqrt{\frac{8k}{27\epsilon_0 W w}} g_0^3 \quad (5)$$

where k is the effective spring constant of the membrane, W is actuation area in center, w is the membrane width, ϵ_0 is the permittivity of free space, and g_0 is the gap height.

The equivalent circuit of unit cell of phase

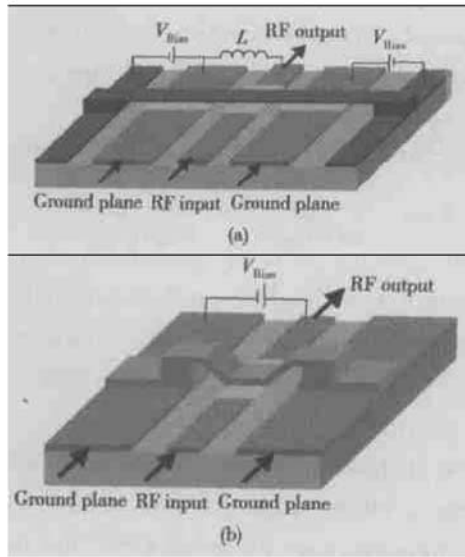


Fig. 2 (a) CPW-actuation configuration; (b) Conventional configuration

shifter is shown in Fig. 3. The series C_{cent} and C_g act as the loaded capacitance C_b . C_{cent} is the capacitance between bridge and central conductor of CPW transmission line, while C_g is capacitance between bridge and ground plane of CPW transmission line. C_b is derived by:

$$C_b = 2 \frac{C_{cent} C_g}{C_{cent} + 2C_g} \quad (6)$$

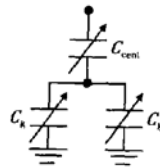


Fig. 3 Equivalent circuit model of unit cell

Accordingly, the bridges are designed to be $50\mu\text{m}$ wide, $360\mu\text{m}$ long and suspended at a height of $3\mu\text{m}$ above the substrate. Theoretic calculation and simulation by Anilent ADS show that 2bit phase shifter have $0^\circ/22.5^\circ/45^\circ/67.5^\circ$ phase shift at 15GHz .

The biasing of each bit is achieved using a single high-resistance line of $15\mu\text{m}$ width, which is attached to one of the bridges in each bit, and all other bridges in the same bit are linked together using meandering high-resistance lines (see Fig. 4).

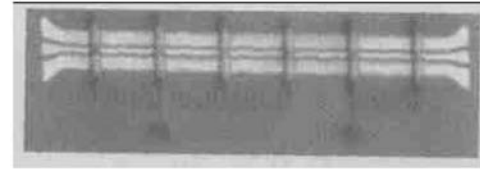


Fig. 4 SEM photograph of the fabricated 2bit MEMS phase shifter

3 Fabrication

The 2bit phase shifter is fabricated on a $350\mu\text{m}$ thick silicon substrate ($\epsilon_r = 11.9$, $\tan\delta = 0.005$, resistivity = $4000\Omega \cdot \text{cm}$). The fabrication process is shown in Fig. 5. A $1\mu\text{m}$ -thick insulating thermal oxide using as a buffer layer is grown on the substrate. Lift-off process is used to define a Cr/Au CPW transmission lines with a thickness of

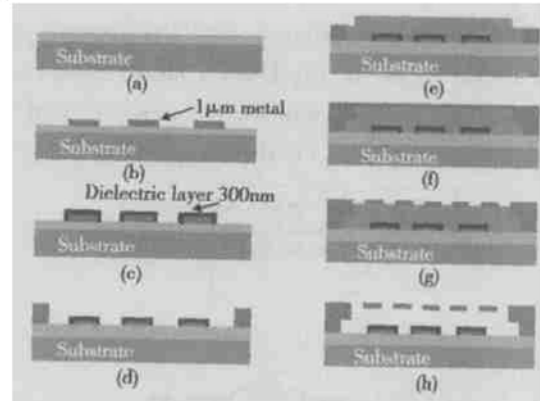


Fig. 5 Details of the fabrication process for the MEMS phase shifter

$1\mu\text{m}$. A $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ layer ($100/50/100\text{nm}$) are grown and patterned on the top of CPW line to form the dielectric layer under bridge. A $4\mu\text{m}$ -thick layer of aluminum alloy is evaporated and patterned to define the bias lines and the mechanical support posts for the switch. A $3\mu\text{m}$ -thick polymer sacrificial layer is spinning coated and patterned. An aluminum membrane layer less than $0.5\mu\text{m}$ thick is deposited and patterned to define the switch membrane. The sacrificial layer is removed by plasma ashing to release the membrane. The SEM photograph of the fabricated 2bit MEMS phase shifter is shown in Fig. 4.

4 Result

The DMTL phase shifter is measured using an HP8510C network analyzer and a SUMMIT 10000 probe station. A line-reflect-match (LRM) calibration was performed using on-wafer standard. The two-port s -parameters of the circuit were recorded up to 36GHz. The pull-down voltage of MEMS switch was measured to be 15V. 20V bias voltage was adopted in our measurement.

The differential phase shift as a function of frequency for all the four switching states is illustrated in Fig. 6(a). It is seen the phase shift increases linearly with frequency up to 32GHz. The evident non-linearity appears at frequency above 32GHz. The measured phase shift is shown in Table 1. It is seen the results are less than the designed phase shift. It is proposed that the bridges can not contact the underneath dielectric layer completely because the gap between the ground of CPW and the anchor of bridges is too short. For this reason, the down-state capacitance is less than the designed one.

Table 1 Phase shift of two-bit phase shifter at 15GHz and 20GHz

| Frequency | 15GHz | | | | 20GHz | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Designed | 0° | 22.5° | 45.0° | 67.5° | 0° | 28° | 54° | 82° |
| Measured | 0° | 11.6° | 32.6° | 48.5° | 0° | 20.1° | 41.9° | 68.2° |
| Phase error | 0° | 10.9° | 12.4° | 19° | 0° | 7.9° | 12.1° | 13.8° |

The change of insert loss to frequency is shown in Fig. 6(b). Insertion loss increases quickly with frequency over 32GHz and is less than -1.8dB in 0~32GHz. The return loss is shown in Fig. 6(c) and less than -1.1dB in 0~32GHz. The ripple in insertion loss can be explained by the inevitable nonuniformities of the load capacitance C_b .

5 Conclusion

The CPW-actuation configuration was proposed for the first time in the distributed MEMS transmission line (DMTL) phase shifter. The bias

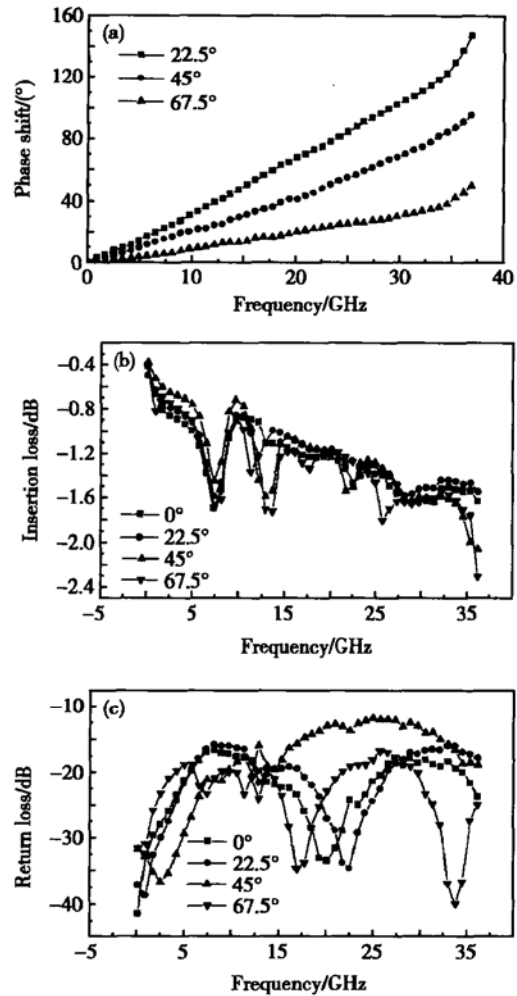


Fig. 6 Measured results of 2bit DMTL phase shifter in all states (a) Phase shift; (b) Insertion loss; (c) Return loss

voltage is less than 20V. A phase shift of 68.2° with an insertion loss less than -1.2dB at 20GHz is demonstrated. In next work, the match between different bits will be considered to reduce the return loss and increase the phase shift of unit cell; the width of central conductor of CPW line will be increased to reduce the insertion loss.

References

- [1] Barker N S, Rebeiz G M. Distributed MEMS true-time delay phase shifter and wide-band switches. *IEEE Trans Microw Theory Tech*, 1998, 46(11): 1
- [2] Borgioli A, Liu Yu, Nagra A S, et al. Low-loss distributed MEMS phase shifter. *IEEE Microw Guided Wave Lett*, 2000,

- 10(1): 7
- [3] Hayden J S, Rebriz G M. 2-bit MEMS distributed X-band phase shifters. IEEE Microw Guided Wave Lett, 2000, 10(12): 540
- [4] Rodwell M J, Allen S T, Yu R Y, et al. Active and nonlinear wave propagation devices in ultrafast electronics and optoelectronics. Proc IEEE, 1994, 82(7): 1037
- [5] Muldavin J B, Rebeiz G M. High isolation CPW MEMS shunt switches-part 1: modeling. IEEE Trans Microw Theory Tech, 1999, 48(12): 1045

一个 DC-32GHz 两位微机械移相器

姜建忠^{1,2} 赵正平^{2,3} 杨瑞霞² 吕 苗³ 胡小东³

(1 河北大学电子信息工程学院, 保定 071002)

(2 河北工业大学信息学院, 天津 300130)

(3 河北半导体研究所微米纳米中心, 石家庄 050051)

摘要: 采用分布式微机械传输线结构实现了两位移相器, 并且为了减小传输线负载电容和驱动电压首次提出了用共面波导传输线来驱动微机械桥的结构(共面波导驱动结构). 结果显示驱动电压小于 20V, 20GHz 时两位移相器的相移为 0°/20.1°/41.9°/68.2°, 插入损耗为 -1.2dB. 在 DC 到 32GHz 的范围内相移具有良好的线性, 插入损耗小于 -1.8dB, 反射损耗好于 -11dB. 实验结果表明了该结构在高介电常数衬底上制造低插损、宽带数字微机械射频移相器的潜力.

关键词: 微电子机械系统; 移相器; 共面波导驱动结构

EEACC: 2575; 1320; 1350

中图分类号: TN4

文献标识码: A

文章编号: 0253-4177(2004)11-1386-05