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A Novel Polysilicon and Oxide Sandwich Deep Trench with Field Limiting Ring for RF Power Transistors*

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Abstract: A vertical sandwich deep trench with a field limiting ring is proposed to improve the breakdown voltage of power devices and high voltage devices. Simulation result shows that nearly 100% breakdown voltage of the plane junction can be realized.

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1 Introduction

The breakdown voltage is one of the most important characteristics of power semiconductor devices and high voltage devices. It is well known that curvature of junction causes increase in electric field strength at local areas so that a premature breakdown will take place[1]. The curvature of junction for RF devices will bring much lower breakdown voltage due to its shallow junction. Various junction termination techniques, for example, field limiting rings (FLR)[2,3], field plates[4~6], reduced surface field(RESURF)[7], junction terminations extension[8], semi-insulating polycrystalline silicon(SIPOS)[9], have been reported to improve breakdown voltage of semiconductor devices.

In recent years, a deep trench has been widely used in isolation[10,11]. In this paper, we proposed a deep trench, which is filled with a sandwich dielectric between p^+ type region and n type region and is combined with FLR, to eliminate the cylindrical junction and spherical junction completely. In the structure undoped polysilicon is deposited into the middle of silicon oxide in the deep trench to form a lateral sandwich structure of silicon oxide-polysilicon-silicon oxide. Then the breakdown voltage of device with the sandwich deep trench structure is very approximate to that of the plane junction of devices which could get a lower leakage current than that of the normal structure. Additionally, a cut-off frequency can also be improved by reducing the collector junction capacitor. The characteristics of breakdown voltage of device are investigated by using the two-dimensional simulator, ATLAS of SILIVAC Corporation.

2 Breakdown characteristics of a deep trench filled with silicon oxide

The simulation is based on a simple RF BJT. The BJT's parameters are listed as following:

Emitter junction depth is 0.1μm, collector

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junction depth is 0.3μm, concentration of epitaxial n^- layer is $5\times10^{15}cm^{-3}$, the thickness of epitaxial n^- layer is 5.5μm, surface concentration of base is $5\times10^{18}cm^{-3}$, surface concentration of emitter is $1\times10^{20}cm^{-3}$.

The breakdown voltage for a single-sided abrupt junction can be calculated

$$BV \approx 60\times(1\times10^{-16}N_B)^{-0.75}$$

So BV_{CB}^{*} = 101V for $N_c = 5\times10^{15}cm^{-3}$. The BV_{CB}^{*} is the approximate value of the collector junction.

The deep trench of width 1μm and depth 5μm filled with silicon oxide is added to two sides of the BJT. Electric equipotential curve of the device with the deep trench in which silicon oxide is filled is shown in Fig. 1. In the active region, the peak of electric field appears at the border of the active region, near the metallurgical junction. The equipotential lines in active region, however, are relaxed for device with deep trench structure so that breakdown voltage is increased.

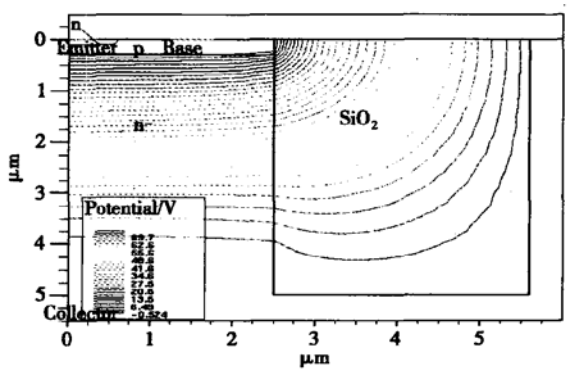

Fig. 1　Potential of deep trench filled in silicon oxide BJT with 1×5μm

The breakdown voltages of device with deep trench are calculated versus trench depth and width. A depth is a key parameter to breakdown voltage for the deep trench structure. It shows that the breakdown voltage of device with 1.2μm deep silicon oxide trench gets almost the same as that of p^+ FLR with same depth by simulation. Apparently, the device with deep trench which is filled with silicon oxide has lower leakage current than the one with p^+ FLR. As we know, it is difficult to fabricate deep p^+ diffusion junction because it will take so long time at very high temperature and increase the defects of the epixatial layer. However, it is easy to form a deep trench by inductively coupled plasma (ICP) etching technique, which has high aspect ratio(HAR).

When the depth of trench filled with silicon oxide is 1.2μm at 1μm width, breakdown voltage is about 54V (when $I_c = 1\times10^{-14}A/\mu m$). While the depth of trench is 5μm, the breakdown voltage is 65.5V. The voltage increases to 79.4V as width increases to 3μm. The wider a trench is, the higher breakdown is, seen in Fig. 2. It can be found that the equipotential electric lines in the trench can relax and smooth those lines in the active region. So a wider trench FLR will provide a higher breakdown voltage. When the width of trench reaches over 2.5μm, saturation phenomenon of breakdown voltage appears. As the trench becomes too wider, the equipotential lines in the trench will be much more relaxant than those in the active region. The wider trench has less effect on smoothing equipotential lines in the active region, so the saturation phenomenon appears.

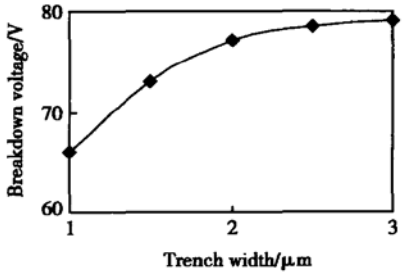

Fig. 2　Breakdown voltage versus width of trench

3　Polysilicon and silicon oxide sandwich deep trench FLR

The breakdown voltage increases as the increase of width of the deep trench . The wider the deep trench, the higher breakdown voltage. The breakdown voltage is 79.4V for the concentration of epitaxial n^- layer $5\times10^{15}cm^{-3}$, when the width of deep trench is 3μm. The much wider trench will

be required when a higher breakdown voltage is needed, which will bring difficulty in process. It takes a very long time to fill the deep trench and brings much large interior stress after the wafer undergoes the subsequent high temperature processes. The interior stress will induce many defects in crystal and decrease reliability of device. Therefore undoped polysilicon is filled between both sides of silicon oxide in the deep trench to overcome the shortcoming. The stress of substrate will be reduced because thermal expansion coefficient of silicon is similar to that of polysilicon, and the breakdown voltage will be increased for the sandwich structure. The electric equipotential distribution is shown in Fig. 3. The parameters of the new structure are 2μm for width of the whole trench, 1μm for the width of the polysilicon, 5μm for the depth of the whole trench, and the rest parameters are the same as those of the deep trench filled with silicon oxide.

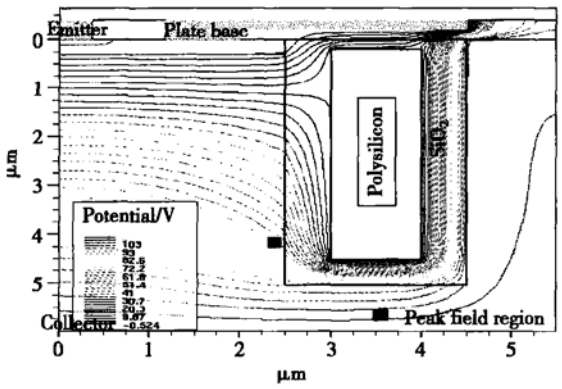

Fig. 3 Potential in BJT of sandwich deep trench with FLR

The whole polysilicon is an equipotential body in the trench, as shown in Fig. 3. The electric equipotential divides the oxide into two parts: on the top and bottom of silicon oxide. By simulation, we find the sandwich deep trench structure filled with polysilicon and oxide can realize much higher breakdown voltage than a deep trench only filled with silicon oxide. When the sustained voltages which are divided by top and bottom of silicon oxide are in the optimum proportion, the electric field in the metallurgical junction region will be decreased and the breakdown point will be moved down toward the bottom of active region, seen in Fig. 3. The premature breakdown at the metallurgical junction region is restrained.

Polysilicon, silicon oxide, and epitaxial layer compose MOS structure. Holes, most of which contribute to the avalanche current are produced in the region of n^- epitaxial region near trench. The higher electric field produced by the crowd equipotential lines at collector junction trends to accelerate these holes in the same area where the breakdown occurs. The holes can pick up sufficient energy to overcome the energy barrier between the interface of silicon and oxide, and be injected into the silicon oxide where some of them will be trapped[12]. So the field decreases and the breakdown voltage increases to compensate for the trapped positive charge.

The field plate is placed on top of the deep trench. It is because when high reverse voltage is supplied, polysilicon becomes "electron trap" due to MOS phenomenon. The reverse voltage in the polysilicon greatly increases the voltage sustained by the silicon oxide. So field plate should be added to release the reverse voltage in the polysilicon body. By simulation, we find the breakdown is not sensitive to the length of the field plate; the length overlapping the polysilicon is enough.

So we aim to reach the optimum proportion of the voltages sustained by top oxide and bottom oxide by adjusting the thickness of top oxide and bottom oxide. See in Fig. 4, 0.2μm thick top oxide is the optimum value in consideration of breakdown voltages($I_c = 1\times10^{-14}$A/μm). It seems the thinner silicon oxide in the bottom will bring advantages because the lateral influence will be reduced. But it will increase the electric field in this region. The breakdown will take place in the silicon oxide if the silicon oxide in the bottom is too thin. The leakage current along the lateral and the bottom border will also increase. When the thickness in the bottom of silicon oxide reaches 100% depth of trench,

the device comes back to the case with only oxide filling deep trench. We find that the thickness of the silicon oxide in the bottom of trench is 20% ~ 30% of the depth of the whole trench is the optimum case. In this case, the breakdown voltage is the highest and the leakage current is medium.

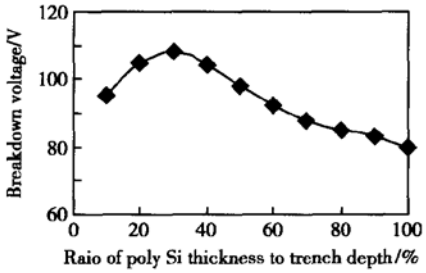

Fig. 4　Breakdown voltage of devices versus top thickness

So we get the optimum parameters: 0.2μm thick top oxide and 1μm thick bottom oxide. By simulation, the device with these parameters realizes 105V of breakdown voltage (I_c= 1×10^{-14}A/μm). This breakdown voltage is 104% to BV^{*}_{CB}.

4 Conclusion

We presented a novel sandwich structure of a deep trench combining with field limiting ring to improve the breakdown voltage of RF power BJT. When using 2 or 3μm wide and 5μm deep silicon oxide trench, the breakdown voltage will increase to around 79% of that of plane junction. And when we add polysilicon and silicon oxide sandwich in the deep trench FLR, the depth of the trench is no longer the only decisive parameter. We realize close to 100% breakdown voltage of plane junction due to the field at metallurgical junction being restrained by voltage division in oxide and the walk-out phenomenon at the metallurgical junction. The results presented are almost independent of the epitaxial layer thickness and the junction depth.

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射频功率晶体管的多晶硅二氧化硅夹心深槽场限制环新结构*

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摘要: 提出一种二氧化硅/多晶硅/二氧化硅夹心深槽场限制环新结构来提高晶体管的击穿电压. 模拟结果显示, 该结构可以使射频功率双极性晶体管的击穿电压几乎 100% 达到平行平面结的理想值.

关键词: 击穿电压; 场限制环; 射频功率器件; 夹心槽
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