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Optimal Stack Generation for CMOS Analog Modules with Parasitic and Mismatch Constraints*

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Abstract: The performances of analog circuits depend greatly on the layout parasitics and mismatches. Novel techniques are proposed for modeling the distributed parasitic capacitance, parasitic parameter mismatch due to process gradient and the inner stack routing mismatch. Based on the proposed models, an optimal stack generation technique is developed to control the parasitics and mismatches, optimize the stack shape and ensure the generation of an Eulerian graph for a given CMOS analog module. An OPA circuit example is given to demonstrate that the circuit performances such as unit gain bandwidth and phase margin are enhanced by the proposed layout optimization method.

Key words: analog constraints; analog circuits layout; stack generation
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1 Introduction

With the remarkable evolution of VLSI technology, mixed analog/digital circuits have been found more and more useful in IC industry. Due to the tight performance needed and the rapid technology innovation rate, the design of the analog parts in mixed signal systems has become an expensive bottleneck. In the past decade, many efforts have been made to increase the automation of the layout design of analog circuits[1—3]. To obtain high performances circuit, control of parasitic capacitance and minimization of the layout mismatch are very crucial[4,5]. In a typical CMOS process, the absolute parametric accuracy of components such as transistors, capacitors and resistors, varies within ± 20%, while the parametric ratios within ± 0.1%[6]. For this reason, the implementation of analog circuit typically relies on component matching rather than absolute accuracy. Moreover, reducing parasitic capacitance can improve the frequency performance of analog circuits in terms of bandwidth and phase margin[7].

The stacking technique[8] is widely used to improve the circuit performance in CMOS analog layout. Merging the diffusion regions of two or more MOS transistors with a common node, we observe that stack can reduce not only the layout area but also the parasitic diffusion capacitance and the component mismatches. Different approaches[1,8—11] of the stack generation have been investigated. A fully stacked layout was first introduced[8] and later on has been widely used in the anglog physical implementation. The stack generator presented in Reference[1] can enumerate all the possible stacks

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with their respective exponential computational complexity. An algorithm with $O(n)$ computation complexity was presented in Reference[9], with a minimum stacks generated. The aspect ratio of a generated stack has been optimized successfully[10], and a cost function was used to compare the junction capacitance of diffusion regions in different implementations of a stack[11]. However, stack generation problems were rarely studied in the past[1,8—11], such as modeling of the parasitic parameter mismatch due to the process gradient, modeling of the inner stack routing mismatch and simultaneous optimization of the stack shape, area and control of parasitic components. The performance of a stacked layout could not be controlled nor optimized without accurate modeling of parasitics and mismatches.

In this paper, novel techniques for the parasitic and mismatch modeling during the optimal stack generation have been proposed, with which, a new transistor folding technique and a dummy transistor insertion technique are further developed to generate optimal stacks for a given diffusion graph. In section 2, the distributed parasitic capacitance model and dummy insertion technique are derived. We present the mismatch modeling technique in section 3. The new technique for the simultaneous optimization of stack shape and control of parasitics is presented in section 4.

2 Modeling of Parasitic Capacitance

In most analog cell circuits, differential pair, current mirror and cascode structure are the basic building blocks, during the layout generation, which can be stacked as basic modules by finding an Eulerian trail[13] in the diffusion graph[1]. The distributed parasitic capacitance in these basic modules is analyzed in this section.

2.1 Unit Parasitic Diffusion Capacitance

The parasitic capacitance of a unit diffusion area towards the substrate or well is calculated in Eqn. (1), which employs the SPICE pn-junction side-wall and plate capacitance model[5].

$$C_{\text{unit}}(N) = \frac{W}{N} L_a C_{jc} + 2\left(\frac{W}{N} + L_a\right) C_{jcsw} \qquad (1)$$

where C_{jc} is the zero-biased source (or drain) capacitonce to substrate (or well) pn-junction unit area plate, C_{jcsw} is that to the substrate (or well) pn-junction unit length side-wall. As shown in Fig. 1, L_a is the length of the unit active area. W/N is the width of the unit active area, where W is the width of the transistor and N is the folding number of the gate.

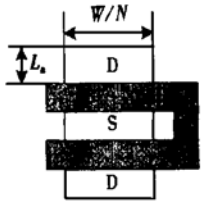

FIG. 1 Unit Parasitic Diffusion Capacitance in Folded Transistor

2.2 Parasitic Capacitance in Single Transistor

If a node in diffusion graph is the end point of the Eulerian trail, it belongs to the external node set EXT, otherwise it belongs to the external node set INT. For a single transistor in Fig. 1, if the gate folding number N is an odd number, the source and drain nodes in the diffusion graph have odd degrees. Both the source and drain nodes are the end points of the Eulerian trail, so they are assigned to the external node set EXT, while the internal node set INT is kept empty. The source or drain parasitic capacitance $C_i(N)$ is thus calculated by Eqn. (2).

$$C_i(N) = \frac{N+1}{2} C_{\text{unit}}(N) \qquad \text{for node } i \in \text{EXT} \qquad (2)$$

If the gate folding number N is even, either the source or drain node is assigned to the external node set EXT or the internal node set INT. The source or drain parasitic capacitance $C_i(N)$ is thus calculated by Eqn. (3).

$$C_i(N) = \begin{cases} \frac{N}{2} C_{\text{unit}}(N) & \text{for node } i \in \text{INT} \\ \left\lceil \frac{N}{2} + 1 \right\rceil C_{\text{unit}}(N) & \text{for node } i \in \text{EXT} \end{cases} \tag{3}$$

2.3 Parasitic Capacitance in Current Mirror

Figure 2(a) shows a current mirror circuit composed of one reference transistor M_0 and k mirrored transistors $M_1, M_2, \cdots, M_k$. All transistors are assumed to have the same channel lengths. The channel width of each transistor $M_j (j = 0, 1, \cdots, k)$ is β_j times of W. W is the channel width of the reference transistor and β_j is the size ratio of the mirror transistor M_j to the reference transistor M_0, specifically we set that $\beta_0 = 1$. Suppose the gate of transistor M_0 is folded by an integer number N, the gate folding number of the mirrored transistor M_j is therefore $\beta_j N (j = 0, 1, \cdots, k)$, which is assumed to be on integer. The corresponding diffusion graph of the current mirror is shown in Fig. 2(b), where the source node S has degree of $\beta_s N = (\beta_0 N + \beta_1 N + \cdots + \beta_k N)$ and each drain node D_j has degree of $\beta_j N$.

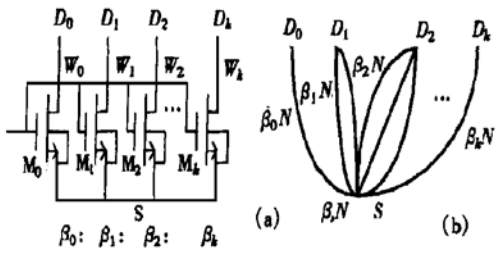

FIG. 2 Current Mirror (a) Circuit Schematic Graph, (b) Diffusion Graph

Dummy Insertion Technique

The diffussion graph in Fig. 2(b) is not always an Eularian graph. Under this circumstance, dummy edges[1] are needed to be added in the diffusion graph to construct the Eulerian graph. Here is a new dummy insertion technique to form an Eulerian graph. Supposing we have node set $V(D_0, D_1, \cdots, D_k, S)$, we construct another two node sets ODD and EVEN by node degrees. Initially all odd-degree nodes in V are moved into set ODD, while all even ones are into set EVEN.

(1) If the folding number N is an even number, every node in diffusion graph has even degree. Thus we set that EVEN contains all the nodes on diffusion graph and ODD is empty. Based on the property of the Eulerian graph[12], at least one Eulerian trail can be found for this diffusion graph.

(2) If N is an odd number, keep only two drain nodes left in set ODD. Each of the rest of drain nodes in set ODD is added with one dummy edge and moved to set EVEN. After the drain node assignment, the source node S is always of an even degree and assigned to set EVEN. In this way, the diffusion graph finally has two odd degree nodes only and one Eulerian trail can be generated[12]. After dummy insertion, each drain node D_i in the new diffusion graph has a new degree of $\overline{\beta_i N}$, which can be calculated by Eqn. (4). The new degree of source node S is given by Eqn. (5).

$$\overline{\beta_i N} = \begin{cases} \beta_i N & \text{for node } D_i \in \text{set EVEN} \\ \beta_i N + 1 & \text{for node } D_i \in \text{set ODD} \end{cases} \tag{4}$$

$$\overline{\beta_s N} = \sum_{i=0}^{k} \overline{\beta_i N} \tag{5}$$

Parasitic Capacitance Calculation

By summing of all the unit diffusion parasitic capacitance connecting to node D_i, the total parasitic capacitance $C_i(N)$ of drain node D_i can be calculated by Eqn. (6). Similarly the source node S parasitic capacitance $C_s(N)$ can be obtained by Eqn. (7). INT and EXT are the internal and external node set of the stack. $C_{\text{unit}}(N)$ is the capacitance of a unit active area calculated by Eqn. (1). Obviously, the parasitic capacitance is a function of the folding number of the reference transistor.

$$C_i(N) = \begin{cases} \frac{\overline{a_i N}}{2} C_{\text{unit}}(N) & \text{for node } D_i \in \text{INT} \\ \left\lceil \frac{\overline{a_i N} + 1}{2} \right\rceil C_{\text{unit}}(N) & \text{for node } D_i \in \text{EXT} \end{cases} \tag{6}$$

$$C_s(N) = \begin{cases} \frac{\overline{a_s N}}{2} C_{\text{unit}}(N) & \text{for node } S \in \text{INT} \\ \left\lceil \frac{\overline{a_s N} + 1}{2} \right\rceil C_{\text{unit}}(N) & \text{for node } S \in \text{EXT} \end{cases} \tag{7}$$

2.4 Parasitic Capacitance in Cascode Structure

Figure 3(a) shows another basic building block circuit, namely a cascode structure. Since the circuit is fully symmetry, we only calculate the parasitic capacitance in the left part of it. Suppose transistor M_r has the minimum channel width W among all the transistors $M_j(j=0,\cdots,k)$, we choose M_r as the reference transistor. The gate folding number of M_r is N. The channel width of each transistor $M_j(j=0,\cdots,k)$ is $\beta_j W$, where β_j is the size ratio of transistor M_j to the reference transistor M_r. We assume all $\beta_j N$ $(j=0,1,\cdots,k)$ are integers. The corresponding diffusion graph is shown in Fig. 3(b), where node S has degree of $\beta_s N = 2\beta_0 N$ and node D_j has degree of $\beta_j N + \beta_{j+1} N$, provided that $\beta_{k+1}=0$.

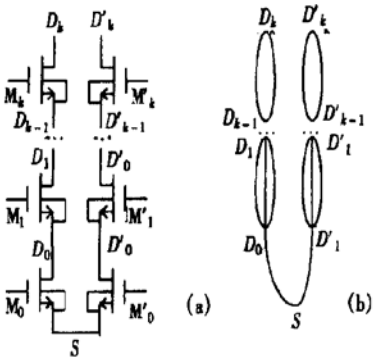

FIG. 3 Cascode Structure (a) Circuit Schematic Graph, (b) Diffusion Graph

Repeat the dummy insertion procedure in section 2.3, a new Eulerian graph can be generated. Every node except node S in the new Eulerian graph has a new degree number calculated by Eqn. (4), that of node S is given in Eqn. (8). In the same way, the parasitic capacitance $C_i(N)$ of node D_i and the parasitic capacitance $C_s(N)$ of node S can be calculated by Eqn. (9) and Eqn. (10) respectively.

$$\overline{\beta_s N} = 2\,\overline{\beta_0 N} \tag{8}$$

$$C_i(N) = \begin{cases} \dfrac{\overline{\beta_i N} + \overline{\beta_{i+1} N}}{2} C_{\text{unit}}(N) & \text{for node } D_i \in \text{INT} \\ \left\lceil \dfrac{\overline{\beta_i N} + \overline{\beta_{i+1} N} + 1}{2} \right\rceil C_{\text{unit}}(N) & \text{for node } D_i \in \text{EXT} \end{cases} \tag{9}$$

$$C_s(N) = \begin{cases} \dfrac{\overline{\beta_0 N} + \overline{\beta_0 N}}{2} C_{\text{unit}}(N) & \text{for node } S \in \text{INT} \\ \left\lceil \dfrac{\overline{\beta_0 N} + \overline{\beta_0 N} + 1}{2} \right\rceil C_{\text{unit}}(N) & \text{for node } S \in \text{EXT} \end{cases} \tag{10}$$

2.5 Parasitic Capacitance in Differential Pair

A differential pair, as shown in Fig. 4, can be regarded as a special case of either the current mirror or the cascode structure. The parasitic capacitance of a differential pair can be calculated by Eqns. (6) and (7), provided that $k=1$, $\beta_1=1$, or by Eqns. (9) and (10) when $k=0$.

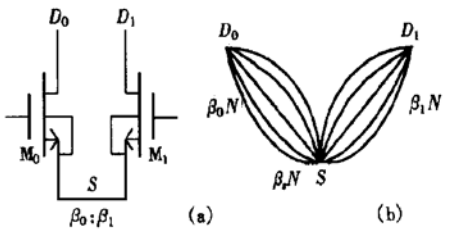

FIG. 4 Differential Pair (a) Circuit Schematic Graph, (b) Diffusion Graph

3 Modeling of Mismatch

In the stack implementation of a pair of matched modules, for every matched transistors, the mismatch in gate capacitance or diffusion parasitic capacitance, which exists in the non-equal length inner stack routing of a pair of matched

nets, can be caused by a process gradient. In order to model these mismatches, we introduce the following parameters.

3.1 Mismatch Parameters for Process Gradient

Assume a pair of matched modules T and T' contain K pieces matched gate nodes which are divided into two matched node sets VG ($v_{g1}, v_{g2}, \cdots, v_{gK}$) and VG$'$($v_{g1}', v_{g2}', \cdots, v_{gK}'$), and J pieces of matched diffusion nodes that are divided into VD ($v_{d1}, v_{d2}, \cdots, v_{dJ}$) and VD$'$($v_{d1}', v_{d2}', \cdots, v_{dJ}'$). Let T_{gk} and $T_{gk}'(k=1, \cdots, K)$ denote the parasitic parameters (such as the parasitic capacitance) of gate v_{gk} and v_{gk}' respectively. Let $\Delta T_{gk} = |T_{gk} - T_{gk}'|$ denote the parasitic parameters mismatch due to process gradient on the matched nodes v_{gk} and v_{gk}'. Similarly we can define T_{dj} and $T_{dj}'(j=1, \cdots, J)$ to be the parasitic parameters of diffusion node v_{dj} and v_{dj}', while $\Delta T_{dj} = |T_{dj} - T_{dj}'|$ be the parasitic parameters mismatch of the matched diffusion nodes due to the process gradient.

3.2 Mismatch Parameters for Wire Length

L_{gk} and $L_{gk}'(k=1, \cdots, K)$ denote the wire lengths of gate nets v_{gk} and v_{gk}' respectively. $\Delta L_{gk} = |L_{gk} - L_{gk}'|$ denote the wire length mismatch between net v_{gk}. and v_{gk}'. Similarly, L_{dj} and L_{dj}' denote the wire length of diffusion nets v_{dj} and v_{dj}' ($j=1, \cdots, J$), and $\Delta L_{dj} = |L_{dj} - L_{dj}'|$ denotes their wire length mismatch.

3.3 Mismatch Function

The mismatch function of the matched modules of T and T' is formulated in Eqn. (11).

$$f(T, T') = \sum_{k=1}^{K} W_{gk}\Delta T_{gk} + \sum_{j=1}^{J} W_{dj}\Delta T_{dj} + \sum_{k=1}^{K} W_{gk}'\Delta L_{gk} + \sum_{j=1}^{J} W_{dj}'\Delta L_{dj} \quad (11)$$

where $W = (W_{gk}, W_{dj}, W_{gk}', W_{dj}')$ are the weight coefficients. If the weight value increases, the corresponding mismatch parameters will affect the circuit performance more significantly. During the optimal stack generation, the value of the mismatch function should be minimized in order to decrease the layout mismatch.

3.4 A Modeling Example: Differential Pair

In this sub-section, a example of differential pair is given to illustrate the above mismatch model. In Figure 5, a comparison is drawn between three symmetry stack implementations in Figure 4 of a differential pair. For the Type-A , the edges of transistors M_1 and M_2 in Figure 4(b) are interleaved in the stack as shown in Figure 5(a) or 5(a$'$). For Type-B, , all of the edges of transistor M_1 are placed on the left of those of M_2 in the stack (as shown in Figure 5(b) or 5(b$'$). The edge placement method in Type-C is shown in Figure 5(c) or 5(c$'$), which is a trade-off between the previous two implementations.

Given a uniform process gradient, we can estimate the mismatch of two gate capacitances (ΔT_g), the mismatch of two drain parasitic capacitances (ΔT_d), the mismatch of two gate routing wire lengths (ΔL_g) and the mismatch of two drain routing wire length (ΔL_d). Table 1 presents the mismatch parameters of transistor M_1 and M_2 in Type-A, Type-B and Type-C implementations. The distance between two adjacent gate stripes in the stacked layout is doneted by a gate unite distance. And the distance between two adjacent drain stripes in the stacked layout, is denoted by a drair unite distance.

In Table 1, Δx is the gate capacitance variation per gate unit distance and Δy is the drain capacitance variation per drain unit distance. Take Type-A for example, the mismatch of two gate capacitances due to process gradient, ΔT_g, is that $(1+2+5+6+9)\Delta x - (0+3+4+7+8)\Delta x = \Delta x$ and the mismatch of the drain capacitance due to process gradient, ΔT_d, is $(2+6+10)\Delta y - (0+4+8)\Delta y = 6\Delta y$. The mismatch of two gate routing wire lengths (ΔL_g) and the mismatch of two drain routing wire length (ΔL_d) are both zero due to the symmetry routing. From Table 1, we can see that Type-A is the best realization, Type-B is the worst

one, and Type-C is a trade-off between A and B, in terms of matching properties.

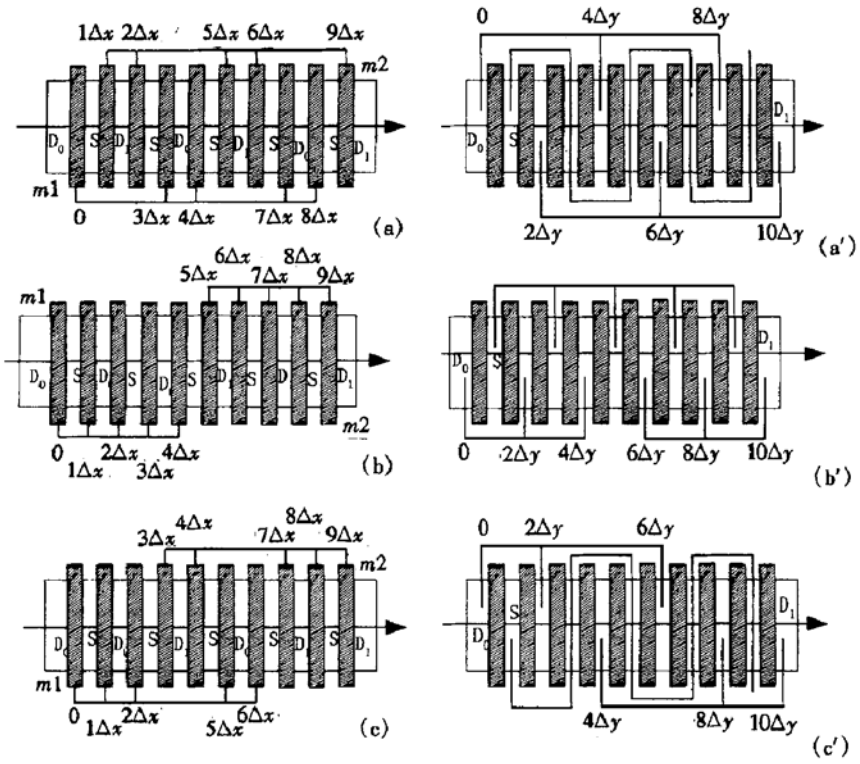

FIG. 5 Three Type Implementations of Differential Pair

Table 1 Mismatch Parameters of Transistor M_1 and M_2 in Type-A, Type-B and Type-C Implementations

	Type-A	Type-B	Type-C
ΔT_g	Δx	$25\Delta x$	$17\Delta x$
ΔT_d	$6\Delta y$	$18\Delta y$	$14\Delta y$
ΔL_g	0	0	0
ΔL_d	0	0	0

4 Optimal Stack Generation

In this section, we apply the proposed parasitic capacitance model and mismatch model to the optimal stack generation. A novel transistor folding technique is proposed to simultaneously optimize the stack shape and parasitic capacitance. Also the dummy insertion technique in section 3 is employed to add dummy edges to guarantee an Eulerian graph.

4.1 Stack Generation Algorithm

The proposed stack generation algorithm consists of the following four steps:

Step 1. Partition the diffusion graph G of the circuit into sub-graphs G_i($i=1, 2, \cdots, k$), according to the device type, matching groups and symmetrical structures[13]. Each sub-graph is a diffusion graph of the basic module, such as a single transistor, a differential pair, a current mirror, a cascode structure or a combination.

Step 2. For each sub-graph G_i, the gate folding number N of the reference transistor should be determined by applying the Transistor Folding Technique in section 4.2, for the purpose of balancing the parasitic capacitance constraints, stack aspect ratio requirements and layout design rules. According to the different N, dummy transistors are added using Dummy Insertion Technique in section 2 to ensure an Eulerian graph.

Step 3. When the folding number is decided, the Eulerian trails will be generated using the basic algorithm in Reference[13].

Step 4. If the number of generated Eulerian trails are more than one for each basic module, matching model is applied to choose the best matching implementation using the mismatch function in Eqn. (11).

4.2 Transistor Folding Technique

In the analog layout, folding large transistors can reduce the diffusion capacitance and optimize the aspect ratio of a stack. However, how to choose the folding number to meet with the parasitic and aspect ratio requirements, was rarely discussed in the previous work[1,4,8—11]. In the following, a novel technique is proposed to determine the folding number based on the parasitic capacitance constraints, aspect ratio constraints and layout design rules.

4.2.1 Transistor Folding by Parasitic Capacitance Bound

To satisfy the node parasitic capacitance constraint in Eqn. (12), where $C_{i\text{bound}}$ is the parasitic capacitance bound, the gate folder number N of the reference transistor should satisfy Eqn. (13), where $N_{c\min}(N_{c\max})$ is the lower (upper) bound of the gate folding number with respect to capacitance constraints. Parameters $N_{c\min}$ and $N_{c\max}$ can be easily derived by substituting $C_i(N)$ into Eqn (6, 7) (or Eqn. (9, 10)) into Eqn. (12).

$$C_i(N) \leqslant C_{i\text{bound}} \tag{12}$$

$$N_{c\min} \leqslant N \leqslant N_{c\max} \tag{13}$$

4.2.2 Transistor Folding by Aspect Ratio Requirement

The stack aspect ratio requirement[6] of a single transistor, or a current mirror, or a differential pair is given in Eqn. (14). The aspect ratio requirement of a cascode structure is given in Eqn. (15). Eqn. (16) restricts the gate folding number N of the reference transistor according to aspect ratio requirement in either Eqn. (14) or Eqn. (15)

$$S_{s\min} \leqslant \frac{W/N}{N\sum_0^k \hat{d}_i L_g + (N\sum_0^k \hat{d}_i + 1)L_a} \leqslant S_{s\max} \tag{14}$$

$$S_{s\min} \leqslant \frac{W/N}{2N\sum_0^k \hat{d}_i L_g + 2(N\sum_0^k \hat{d}_i + 1)L_a} \leqslant S_{s\max} \tag{15}$$

$$N_{s\min} \leqslant N \leqslant N_{s\max} \tag{16}$$

where $N_{s\min}(N_{s\max})$ means the lower (upper) bound of the folding number N, which makes the stack aspect ratio meet with lower bound $S_{s\min}$ and upper bound $S_{s\max}$. W and L_g denote the width and channel length of the reference transistor respectively. L_a denotes the length of the unit active area of the module. The numerator and denominator in Eqns. (14) and (15) are the total module width and the total module length respectively.

4.2.3 Transistor Folding by Design Rule

The gate folding number N is also restricted by the design rule in Eqn. (17).

$$N \leqslant N_{d\max} \tag{17}$$

where $N_{d\max}$ means the maximum gate folding number, exceeding which , design rule violations may occur.

The actual folding number of the reference transistor can be determined by the common solutions of the above restrictions in Eqns. (13), (16) and (17). If such a common solution can not be obtained, the folding number should be decided by satisfying the design rule, the performance requirement, and the shape constraints in turn. For any failure in the performance spec can not be satisfied in any case, information of tight performance constraints will be fed back to the circuit designer.

5 Experimental Results

The stacks have been generated for several circuits, among which, OPA circuit and its stacks are prosented in Fig. 6 and 7. We have also simulated the circuit performance by SPICE after extracting the parasitic capacitance and mismatch parameters due to process gradient from the layout. Considering a typical 1% unit capacitance variation from the nominal value due to the uniform process

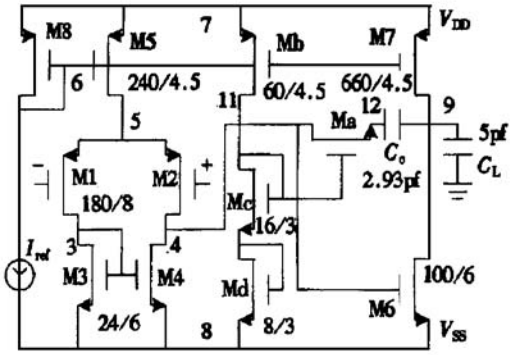

FIG. 6 OPA Circuit

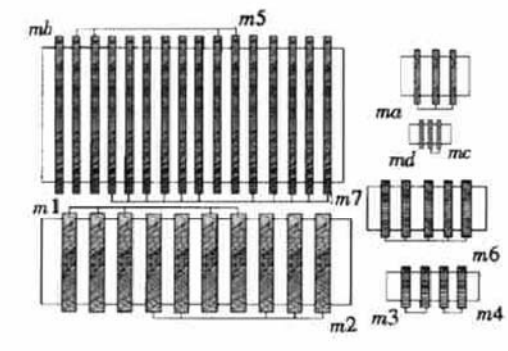

FIG. 7 Generated Stack Modules of OPA

gradient in one unit distance in the layout, we calculate the parasitic capacitance parameters during three implementations of the differential pairs. The SPICE simulation results are listed in Table 2. If the parasitic capacitance of all the transistors except the differential pairs M_1 and M_2 has been calculated, the circuit performance would be obtained in the second column in Table 2. Having added the parasitic capacitance of the differential pairs, we obtain the simulation results of Type-A, Type-B and Type-C implementations in Table 2. It is observe that Type-A implementation has the best circuit performance in terms of the unit gain bandwidth (UGB) and phase margin (PM).

Table 2 SPICE Simulation Results of Three Type Implementations

	No Parasitics	Type-A	Type-B	Type-C
UGB/MHz	4.395	4.382	4.362	4.373
PM	- 117.80	- 118.40	- 120.30	- 119.60

For the same OPA circuit in Figure 6, using the stack generation algorithms and transistor folding technique in section 4, we generate the optimal layout shown in Fig. 8. We also generate another layout (shown in Fig. 9) without any optimization

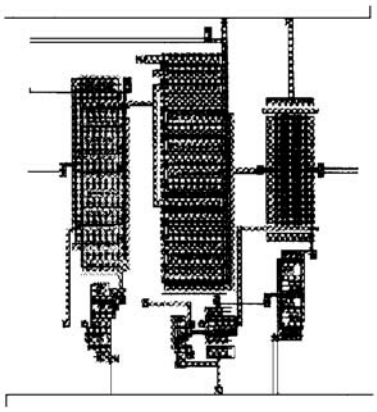

FIG. 8 OPA Optimal Layout

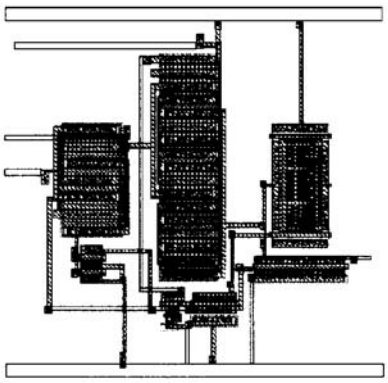

FIG. 9 OPA Layout Without Optimization

of stack shape and parasitic considerations. Table 3 shows the gate folding number of each transistor in Fig. 8 and 9. Table 4 shows the parasitic capacitance of each circuit node in Fig. 8 and 9. The circuit performances with and without the proposed layout optimization are shown in Table 5. It can be seen that after layout optimization, up to 8% unit gain bandwidth enhancement and up to 7% phase margin enhancement are achieved.

Table 3 Gate Folding Number of Each Transistor in OPA Circuit

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_a	M_b	M_c	M_d
Fig. 8	5	5	2	2	4	5	11	2	1	2	1
Fig. 9	3	3	1	1	4	1	11	1	1	1	1

Table 4 Parasitic Capacitance of Each Node in OPA Circuit

	3	4	5	9	10	11	12
Fig. 8	0.322	0.343	0.853	1.075	0.0259	0.1802	0.0381
Fig. 9	0.361	0.398	0.855	1.094	0.0306	0.1825	0.0426

Table 5 SPICE Simulation Results of Two Layout Implementations of OPA

	No Parasitics	Fig. 8	Fig. 9
UGB/MHz	4.571	4.369	4.050
PM	- 110.90	- 115.40	- 122.60

6 Conclusions

In this paper we have discussed the parasitic and mismatch modeling in CMOS stack layout. Our proposed models apply to the proposed models to the simultaneous optimization of stack shape, control of parasitic capacitance and minimization of mismatch due to process gradient and mismatch of inner stack routing. The method has been proved to be correct and efficient by design examples. The SPICE simulation results given in section 5 demonstrate that up to 7% performance improvements have been achieved. However, in our proposed method, the current mirror (or cascode structure) requires the product of the gate folding number N and the size ratio of the mirror transistor (or cascode transistor) to the reference transistor β_j to be integer. In the future research, we intend to extend the proposed method to deal with the none-integer ratio, which exists in many real analog circuits.

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带寄生及匹配约束的 CMOS 模拟电路模块的 STACK 生成优化方法*

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摘要: 模拟电路的性能紧密依赖于版图的寄生参数和匹配特性. 提出了用以描述分布式的寄生电容和由于工艺梯度变化而产生的寄生参数不匹配以及 STACK 内连线的不匹配的模型. 基于该模型, 一种新的 STACK 生成方法用来控制版图的寄生参数和匹配特性, 优化 STACK 的形状和确保为所给出的模拟电路模块生成相映的欧拉图. 一个 OPA 电路的例子说明了所提出的版图优化方法可以提高诸如单位增益带宽和相位余量等电路性能.

关键词: 模拟约束; 模拟电路版图设计; STACK 生成

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