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GeSi Source/Drain Structure for Suppression of Short Channel Effect in SOI p-MOSFET's*

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Abstract: GeSi source/drain structure is purposefully adopted in SOI p-MOSFET's to suppress the short channel effect (SCE). The impact of GeSi material (as source only, drain only or both source and drain) on the threshold voltage rolling-off and DIBL effect is thoroughly investigated, as well as the influence of the Ge concentration and silicon film thickness. The Ge concentration should be carefully chosen as a tradeoff between the driving current and SCE improvement. The detailed physics is explained.

Key words: short channel effect; MOSFET; SOI
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1 Introduction

With the continual scaling down of the device feature size, short channel effect becomes more and more prominent. High channel doping concentration is applied to improve the short channel effect (SCE), but results in the mobility degradation[1—3]. Shallow junction, thin gate oxide and channel engineering can also be used to suppress SCE by trading off the technology limitation, tunneling current and performance optimization[1—3]. GeSi material has been used as the channel to improve PMOSFET performance in terms of transconductance, mobility and cutoff frequency[4—5]. In SOI MOSFET's, GeSi material as source/drain is also used to improve the floating body effect[6]. Yet there is no report on the short channel characteristics for GeSi source/drain structure in SOI MOSFET's. As for p^+ GeSi/n-Si, the band offset in the valence band can reduce the depletion width and the electric flow line penetration. In this paper, the dependence of SCE, in terms of threshold voltage rolling-off and DIBL effect, on the adoption of GeSi material in SOI PMOSFET is investigated using two-dimensional simulation tool MEDICI. The impact of the Ge concentration and silicon film thickness on the improvement of SCE in SOI MOSFET's with GeSi source/drain structure is also evaluated. The related physics is ana-

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lyzed and explained.

2 Simulation

The cross sectional view of the simulated device is shown in Fig. 1. Two-dimensional numerical simulator MEDICI is used. Energy equilibrium equations for both electrons and holes are taken into account, as well as the influence of the lateral and vertical electric field on the carrier mobility. GeSi material as source/drain, is characterized in MEDICI by the necessary material parameters.

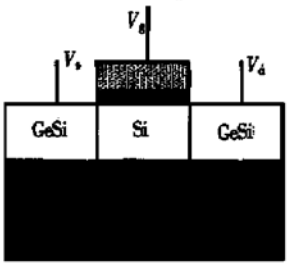

FIG. 1 Cross Sectional View of GeSi Source/Drain MOSFET

In the simulation, the source, body and drain are all assumed to be uniformly doped, which basically satisfies to the SOI devices fabricated by SIMOX materials. The buried oxide thickness and the doping concentration of the source/drain are chosen as 400nm and $1\times10^{20}\,cm^{-3}$, respectively. The gate oxide thickness is chosen as 4nm. Other device parameters will be addressed in the following sections. The threshold voltage is defined as the gate voltage when the drain current reaches 10^{-7} A (W/L) at the drain voltage V_{cc} of 0.05V. The DIBL effect, expressed as the DIBL voltage V_{DIBL}, is the difference in gate voltage between the one acting as the threshold voltage and that producing the drain current of the same magnitude with the applied drain voltage.

Our investigation is focused on the efficiency of SCE suppression by GeSi source/drain structure in terms of the DIBL effect and short channel effect, as well as the dependence of short channel characteristics on the device parameters, such as the Ge concentration and silicon film thickness. The difference in the improvement in the device performance due to the adoption of GeSi material on source only, drain only, or source and drain is also studied.

3 Results and Discussion

Figure 2 gives the comparison between the effectiveness of the adoption of GeSi material with source only, drain only, source and drain for SCE suppression at the drain voltage V_d of − 0.5V. The

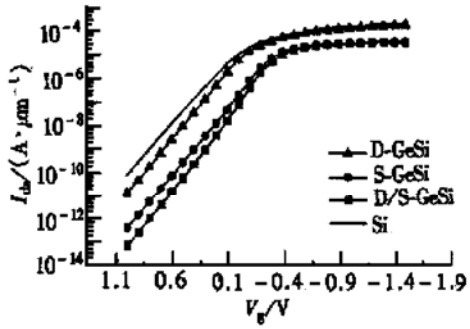

FIG. 2 Transfer Characteristics of MOSFET's with Si Source/Drain, GeSi Source, GeSi Drain and GeSi Source/Drain t_{Si} = 40nm, $N_{ch}=2\times10^{17}\,cm^{-3}$, L = 0.1μm, Ge% = 0.3.

channel length L is 0.1μm. The silicon film thickness t_{Si} and channel doping N_{ch} are 40nm and $2\times10^{17}\,cm^{-3}$, respectively. The Ge concentration is 0.3. It can be seen that GeSi located at the source side is more effective for the SCE improvement than that at the drain side, and GeSi source/drain structure is the most effective one, which is because the discontinuity of valence band results in a high hole barrier at the source side even at a high drain voltage. The energy bands of MOSFET's with Si source/drain and GeSi source/drain at V_d being − 0.05V and − 1V are shown in Fig. 3. The amplified figures explicitly indicate the variation of the hole barrier with the changed drain voltage. Obviously, for p-MOSFET's with GeSi source, the hole barrier shows indistinct reduction at a higher drain voltage in comparison with that in p-MOSFET's with Si source. This clearly explains

the improved DIBL effect in p-MOSFET's with GeSi source/drain structure. This kind of structure is chosen in the following investigation. Yet GeSi source/drain structure is not so effective in n-MOSFET's as that in p-MOSFET due to the small discontinuity of conduction band. GeSi material can be used in the channel region in n-MOSFET to enhance the carrier mobility and the transconductance, as well as alleviate the mobility degradation effect in small dimensional devices. And tradeoff should be made for n-MOSFET's between channel doping, gate oxide and junction depth, etc. to suppress SCE. However, for p-MOSFET's, there exist many problems except that a tradeoff has to be made. For example, p^+-poly gate, instead of n^+-poly gate, should be used to improve SCE, but resulting in the boron penetration. In addition, channel length should be further shortened due to the faster diffusion of boron than phosphorus. Hence, it seems that it is difficult to make the tradeoff for p-MOSFET's for the mitigation of SCE. The adoption of GeSi source/drain structure is one of the good choices for p-MOSFET's.

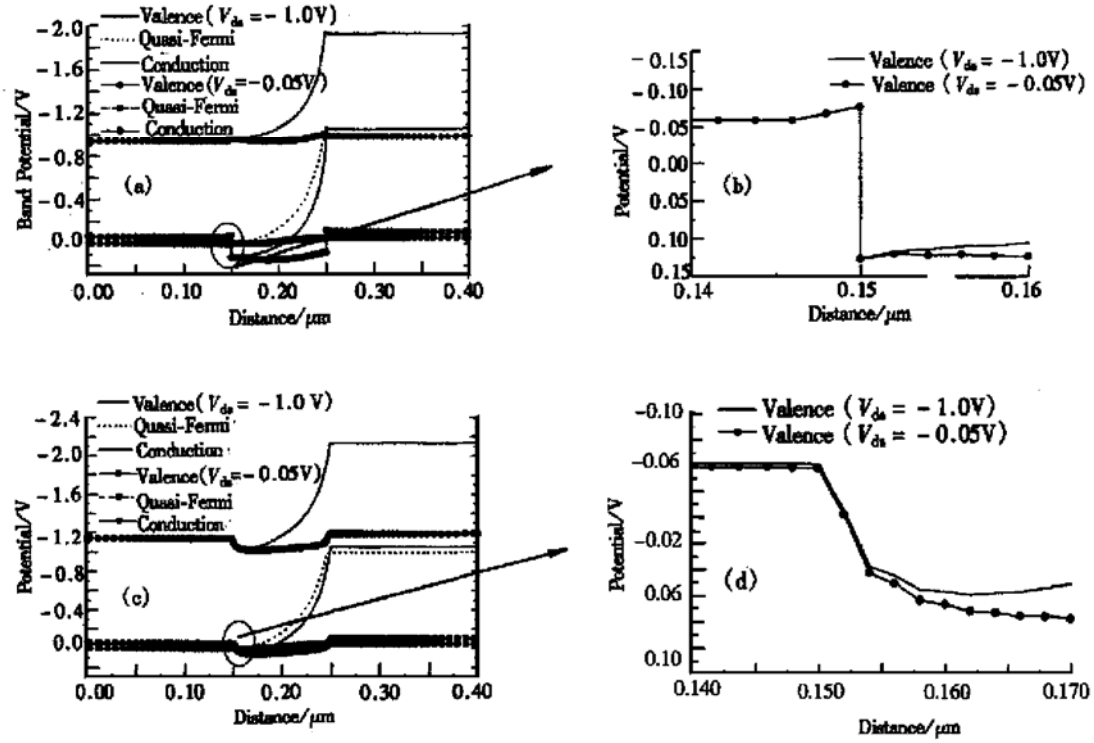

FIG. 3 (a) Energy Band of MOSFET's with GeSi Source/Drain; (b) Amplified Figure of the Specified Region in (a); (c) Energy Band of MOSFET's with Si Source/Drain; (d) Amplified Figure of the Specified Region in (c)

Figure 4 describes the comparisons of the threshold voltage rolling-off with the reduced channel length, as well the DIBL effects between GeSi and Si source/drain structure with t_{Si}= 40nm, $N_{ch} = 2 \times 10^{17}\,cm^{-3}$, Ge%= 0.3. It is noted that compared with that with Si source/drain, MOSFET with GeSi source/drain shows appreciably improved short channel effect in terms of threshold voltage rolling-off and DIBL effect. In this way, GeSi material is adopted in SOI MOSFET's not only for the purpose of suppression of floating body effect, but also for the improvement of SCE. Owing to the higher barrier, GeSi source/drain structure leads to the reduction of drain current in comparison with Si source/drain structure, as shown in Fig. 2. The Ge concentration must be carefully cho-

sen as a tradeoff between the driving current reduction and SCE improvement. Figure 5 illustrates the tradeoff when t_{Si}= 40nm, N_{ch}= $5\times10^{17}cm^{-3}$, L = 0.1μm, and the driving current is estimated as V_g = V_d= − 1.0V. Threshold voltage rolling off is defined as ($V_t(L=0.5\mu m)-V_t(L=0.1\mu m)$). Taking the experimental feasibility into account, Ge concentration can be chosen as 0.2− 0.3 for the tradeoff.

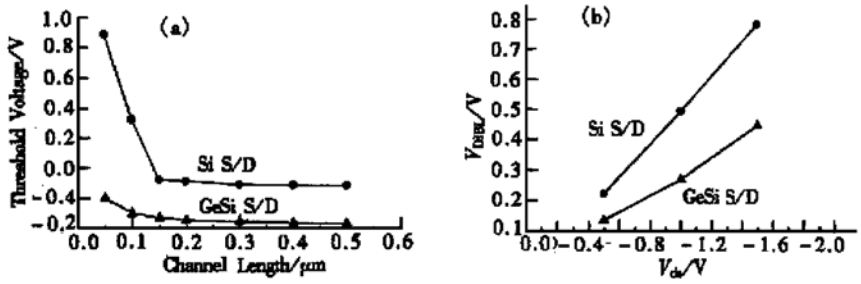

FIG. 4 (a) Comparison of Threshold Voltage Rolling-off with Reduced Channel Length Between GeSi Source/Drain and Si Source/Drain when t_{Si}= 40nm, N_{ch}= $2\times10^{17}cm^{-3}$, Ge% = 0.3; (b) Comparison of DIBL Effect Between GeSi Source/Drain and Si Source/Drain when L= 0.1μm, t_{Si}= 40nm, N_{ch}= $2\times10^{17}cm^{-3}$, Ge% = 0.3

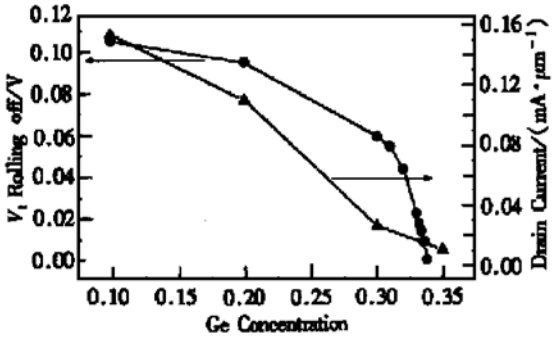

FIG. 5 Trade-off of Ge Concentration Between SCE Improvement and Drain Driving Current when t_{Si}= 40nm, N_{ch}= $5\times10^{17}cm^{-3}$, L= 0.1μm

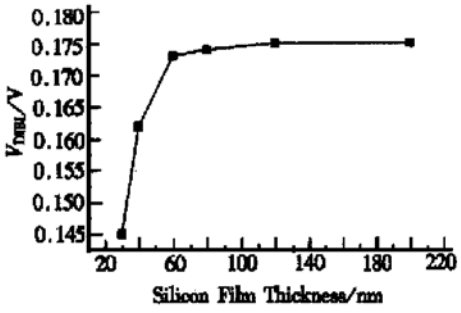

FIG. 6 Influence of Silicon Film Thickness on Improvement of DIBL Effect for GeSi Source/Drain MOSFET's when N_{ch}= $5\times10^{17}cm^{-3}$, L= 0.1μm, Ge% = 0.3

Figure 6 shows the impact of the silicon film thickness on the improvement of DIBL effect in GeSi source/drain MOSFET's when N_{ch}= $5\times10^{17}cm^{-3}$, L = 0.1μm. Similar tendency as Si source/drain has been obtained, i.e., the improvement is more distinct in fully-depleted regime than that in partially-depleted regime, but saturated in partially-depleted regime. This is due to the similar fact of the adoption of shallow junction to suppress the SCE in bulk devices.

4 Conclusion

In this paper we have investigated the efficiency of SCE suppression by GeSi source/drain structure, as well as the dependence of short channel characteristics on some device parameters, such as the Ge concentration, silicon film thickness. The related physics is given qualitatively. In addition, the Ge concentration should be carefully chosen as a tradeoff between the driving current and the SCE improvement.

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抑制 SOI p-MOSFET 中短沟道效应的 GeSi 源/漏结构*

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摘要: 提出在SOI p-MOSFET 中采用GeSi 源/漏结构, 以抑制短沟道效应. 研究了在源、漏或源与漏同时采用GeSi 材料对阈值电压漂移、漏致势垒降低 (DIBL) 效应的影响, 并讨论了Ge 含量及硅膜厚度变化对短沟道效应及相关器件性能的影响. 研究表明Ge 含量应在提高器件驱动电流及改善短沟道效应之间进行折中选择. 对得到的结果文中给出了相应的物理解释. 随着器件尺寸的不断缩小, GeSi 源/漏结构不失为p 沟 MOS 器件的一种良好选择。

关键词: 短沟道效应; MOSFET; SOI

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