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Fabrication of 4H-SiC Merged PN-Schottky Diodes

ZHANG Yu-ming[1], ZHANG Yi-men[1], P. Alexandrov[2] and J. H. Zhao[2]

(1 *Institute of Microelectronics, Xidian University, Xi'an 710071, China*)
(2 *Department of Electrical and Computer Engineering, The State University of New Jersey, NJ 08854-8058, USA*)

Abstract: The design, fabrication and characteristics of 4H-SiC merged PN-Schottky (MPS) diodes with Ni Schottky contact and junction termination extension (JTE) edge termination are reported. A multiple-energy implantation Al in the surface of the n^- drift region below the face-to-face Schottky metal formed pn junctions, which screen the Schottky contact from high electrical, post implantation annealing has been done at 1500℃ for 30min in the ultra-high purity Ar ambient. The devices can block more than 600V reverse voltage and the lowest leakage current at − 600V is 1×10^{-3}A/cm^2, while the forward current density at 3V is more than 200A/cm^2 for 1000μm devices, 1000A/cm^2 at 3.5V for 300μm devices.

Key words: power devices; SiC; semiconductor diode; MPS
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1 Introduction

Silicon carbide(SiC) is a possible candidate to replace the silicon-based devices in the market of high power devices. The potentials of SiC power devices were clearly demonstrated several years ago[1]. The state-of-the-art high voltage power devices have been reviewed in Reference[2]. The highest reverse blocking voltage for a 4H-SiC rectifier reported is about 5000V so far. SiC MOSFETs have been demonstrated lower in the on-resistance than that of the silicon device. At room temperature, the 5000V IGBT and GTO have a lower forward drop than the power MOSFET when the current densities exceed 100A/cm^2. However, at a higher temperature, both the GTO and the IGBT are superior. Experimentally, both n- and p-channel IGBT's have been demonstrated in either 6H- or 4H-SiC up to 800V, but the forward drop is still far from the optimal one. The symmetric and asymmetric 4H-SiC gate-controlled thyristors reported have the breakdown voltage up to 1000V and current-handling capabilities up to 6A.

Both two- and three- terminal devices are needed to construct the basic power circuit units, such as a half-bridge circuit. The most common two-terminal devices are Schottky and PIN rectifiers. The main advantage of a PIN diode is its lower leakage current under the reverse biases, while its disadvantage is that its forward turn-on voltage is inherently higher than that of a Schottky

ZHANG Yu-ming Ph. D, associate professor, was born in 1965. His work includes in novel semiconductor devices, TCAD and VLSI CAD. In particular, his current research interests focus on modeling and simulation, process technologies and devices physics for SiC-based devices.

ZHANG Yi-men male, professor, Ph. D's advisor, was born in 1941. He achieves great attainments in the field of device modeling and simulation in VLSI, VLSI CAD, quantum well devices, IC and high temperature microelectronics in wide band gap semiconductor.

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diode, as is especially true for a wide-bandgap semiconductor SiC. Another problem of the PIN diode is the carrier storage during the on-state, which results in a switching delay when it is driven from the forward conduction to the reverse blocking. On the other hand, a Schottky diode has the advantages of a low turn-on voltage and fast transient recovery. However, due to the Schottky barrier height, the Schottky diode can never achieve the low leakage current of the PIN diode. The well-known Schottky barrier lowering with the image force, which results in an exponential increase of reverse current with the square root of the field strength ($J_R \sim \exp(\sqrt{E})$), is more crucial in SiC due to its extreme high critical electrical field strength (3MV/cm). The increased leakage through the Schottky barrier contact is fairly pronounced at high temperatures, during which the SiC devices are expected to be used.

To combine the best features of these two rectifiers, merged PN-Schottky (MPS) diode with the hybrid rectifier structure has been proposed by Wilamowski[3] for Si and demonstrated by Held *et al.* for SiC[4]. It combines the forward characteristics of the Schottky diode with the reverse property of the PN diode, and the tradeoff in it between the device reverse leakage current and the forward voltage drop can be overcome because the device reverse characteristics are determined by PN junctions of the device instead of the Schottky barrier height. Hence, it is possible to reduce the MPS forword voltage drop by using a tower-barrier contact metal, without increasing the reverse leakage currents.

The principle of MPS has been experimentally demonstrated in SiC[4,5]. However, the fabricated devices have not been optimized with respect to the tradeoff between forward conduction and reverse blocking. Geometrical shapes and junction qualities can be adjusted to fully optimize the device. Advanced termination techniques apply to those devices with the maximum blocking capabilities obtained. So, further study in this problem is desired.

Some papers on SiC material characteristics[5—9] have been reported in China, while few on SiC devices[10—14] have been done. In this paper, the design, fabrication and characterization of 4H-SiC MPS diodes are reported.

2 Design and Fabrication

Figure 1 shows the conceptual illustration of the SiC MPS diode to be investigated in this paper. In this device, the n^- 4H-SiC epitaxial layer is grown on the n^+ 4H-SiC substrate. On the surface of the main device area, p^+ implanted regions alternate with the unimplanted one with spacing of several microns. A Schottky contact is designed to cover both the implanted regions and the unimplanted ones. The substrate ohmic contact being under a positive applied bias, the depletion region will spread from the Schottky interface made by the Schottky contact and the unimplanted region. At the same time, they will also spread from p-n interfaces made by the n^- epitaxial layer and the p^+ implanted regions. At a certain high bias, the depletion regions from the p-n junctions touch each other, as shields the Schottky interfaces from the higher electric fields. Thus, the leakage currents through the Schottky interface are effectively suppressed. When a forward bias is applied, the Schottky interfaces turn on and start to conduct currents at a relatively low bias, which is determined by the Schottky barrier height. Only the ig-

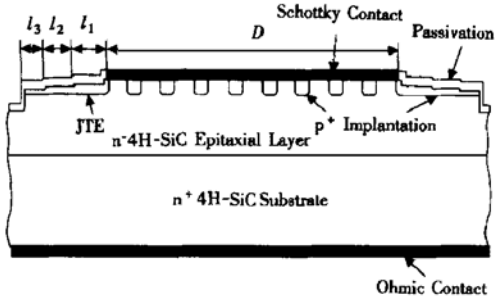

FIG. 1 Schematic Cross-Sectional View of SiC MPS Diode

norable low current flows through the p-n junctions because they will not turn on until a much larger bias is applied. Therefore, the carrier injection from the p^+ regions to the n^- epitaxial layer is kept minimum, assuring the fast reverse transient recovery.

Besides the design of the MPS in the main device area, it is necessary to design the junction termination properly at the periphery of the device to make the reverse blocking voltage close to the breakdown voltage of the planar structure and to suppress the leakage currents along the periphery. In this paper, a new junction-termination-extension (JTE) structure is employed. As shown in Fig. 1, the structure is made by using the same p^+ implantation in the MPS and the subsequent stepwise etchings. Owing to the gradual thinning of the p^+ implantation extension, the reverse bias gradually terminates near the periphery, suppressing the appearance of the very high electric field. In addition, the outmost deeper etching proves the complete termination of the implanted surface. For these devices, a new structure with improved JTE parameters, namely three-step JTE structure, has been used.

Different types of devices were implemented in the mask set. The contact diameter of all types of diodes is either 1000μm or 300μm. The implantation width d is 1.5μm, and the spacing s varies from 2μm to 3μm. For JTE, the widths l_1, l_2 and l_3 are 75, 75 and 50μm, respectively.

Detailed fabrication steps: n^-/n^+ 4H-SiC epitaxial wafers used in the fabrication are purchased from Cree Research, Inc. The thickness and doping concentration of the epitaxial layer are 6μm and $2.3\times10^{16}\,cm^{-3}$, respectively. The thickness and resistivity of the substrate are 35.56μm and 0.018—0.019Ω·cm, respectively. The wafers are of the production grade with low micropipe density of $21cm^{-2}$. The wafers were divided into smaller pieces, and cleaned in the following sequence: acetone with ultrasonic; oxygen plasma cleaning in the ICP chamber; HF 49% for 10min with ultrasonic; $H_2SO_4+H_2O_2$ (4∶1) at 90℃ for 20min.

A multiple-energy implantation Al has been done at room temperature with thick photoresist mask. The implantation conditions are summarized in Table 1. The implantation profile, as simulated by ProfileCode™ (Implant Sciences Corp.), is shown in Fig. 2. The average concentration of the box profile is about $2\times10^{18}\,cm^{-3}$, with a depth of 0.65μm about. The p-n junction depth, which corresponds to the point where the implanted concentration equals the background doping of $10^{16}cm^3$, is about 0.8μm. The actual profile, after the post-implantation annealing is expected to be as deep as 1.0μm.

Table 1　Aluminum Implantation Conditions

	Ion	Energy/keV	Dose/cm^{-2}
1	Aluminum	600	5.2×10^{13}
2	Aluminum	380	3.2×10^{13}
3	Aluminum	235	2.5×10^{13}
4	Aluminum	135	1.6×10^{13}
5	Aluminum	70	9.0×10^{12}
6	Aluminum	30	5.0×10^{12}

Post implantation annealing to activate the implanted Al dopant was done in an ultra-high purity Ar ambient in a conventional furnace at 1500℃ for 30min, during which, the samples were aspectant with the dummy SiC wafers to protect the sample surface. After the annealing, the samples were cleaned by the following procedures in turn: acetone with ultrasonic; oxygen plasma cleaning in the ICP chamber; HF 49% for 10min with ultrasonic; $H_2SO_4+H_2O_2$ (4∶1) at 90℃ for 20min; standard RCA cleaning procedure.

After the implantation and annealing, the edge termination was done on the samples. Firstly, the mesa termination is formed by ICP etching with a 350nm Al etching mask. The etched depth was 3.0μm, and the first, second and third JTE etched depth was 0.29, 0.03, and 0.03μm, respectively. Surface passivation was formed by the thermal oxidation of an oxidized layer of 50nm in thickness and then covered by 1.0μm LPCVD SiO_2 layer. 350nm Ni layer was deposited by sputtering

on the backside and annealed at 1050℃ for 5min in the forming gas (H_2 ∶ Ar= 5% ∶ 95%) to form an ohmic contact. Then the top-side Schottky contact was formed. Ni(100μm) and Al(300nm) were deposited by sputtering and patterned by lift-off in acetone. During that, Ni served as a Schottky contact while Al as an overlay metal.

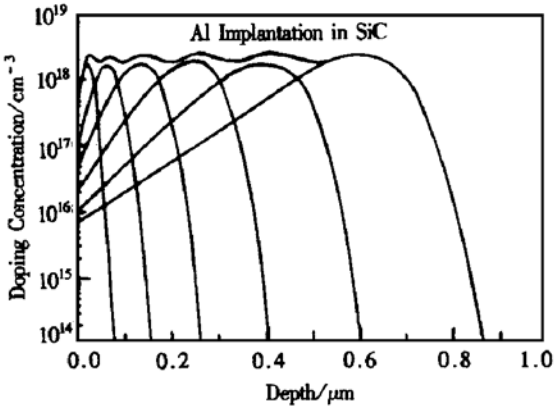

FIG. 2 Simulation Results of Al Implantation in Device Fabrication

3 Device Characterization

For the first time, the fabricated MPS diodes were visually inspected through an optical microscope. Bad devices with defects, such as defects in the original epitaxial wafer and the imperfections of photolithography were rejected, while the rest would be further tested electrically. With devices immersed in Fluorinert™ electronic liquid, the reverse leakage current and the blocking voltage were tested by using a computer controlled test setup, which consisted of a Keithley248 high voltage source and Keithley6517A digital electrometer. The forward characteristics were tested with an HP4145B semiconductor parameter analyzer and Tektronix 371A curve tracer when the devices are exposed to open air. All tests were performed at room temperature.

Figure 3 shows three typical I-V curves for 4H-SiC MPS diodes with diameter 1000μm and Ni Schottky contact ring width being 2μm. It is shown that the leakage current density at − 600V

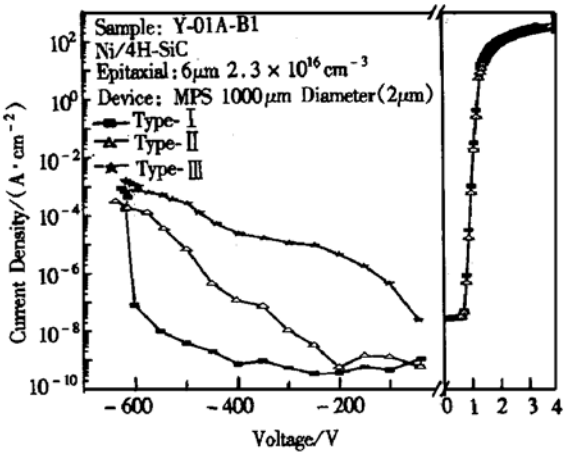

FIG. 3 I-V Characteristics of MPS Diode with 1000μm Diameter and Ni Contact

is less than 10^{-3}A/cm^2. The forward current density at 3V is more than 200 A/cm^2. From the reverse characteristics, we can see that the Type-Ⅰ reverse leakage current is similar to the current of PN diode; type-Ⅲ is more like the Schottky diode, especially when the reverse bias is below 200V; type-Ⅱ is a typical MPS curves as we expected. The reason the leakage currents are different is that the thick photoresists masks for p ring implantation are not uniform and the implantation widths d are various. In any case, the reverse characteristics are determined by the screening effect of the p-n junctions. The Schottky barrier height is not an important factor for the reverse leakage current if the reverse bias is very large. The breakdown voltage of the MPS is about 600V. More than 70% of the parallel plane junction voltage have been achieved, as proves the junction-termination-extension (JTE) structure effective. Many of the big diodes (having a diameter of 1000μm) will break down when the reverse bias is below 50V and the yield is less than 10%, because there are many micropipes in the wafer as well as some defects induced in the process of etching, etc. However, as for the small devices(having a diameter of 300μm), the yield is more than 80%, though the leakage current and the breakdown voltage are almost the same, as is shown in Fig. 4 (a).

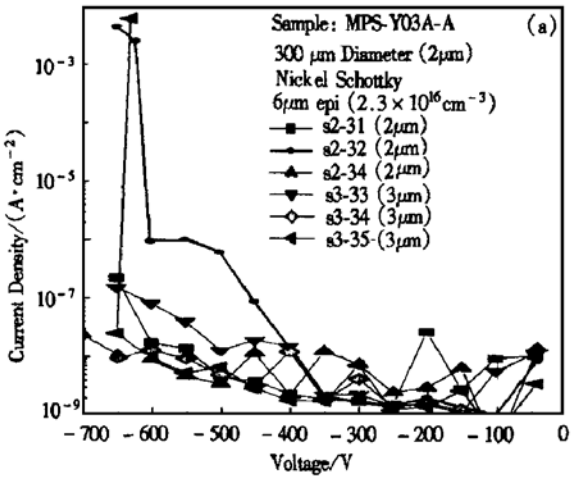

FIG. 4(a)　Reverse Characteristics of MPS Diode with 300μm Diameter and Ni Contact

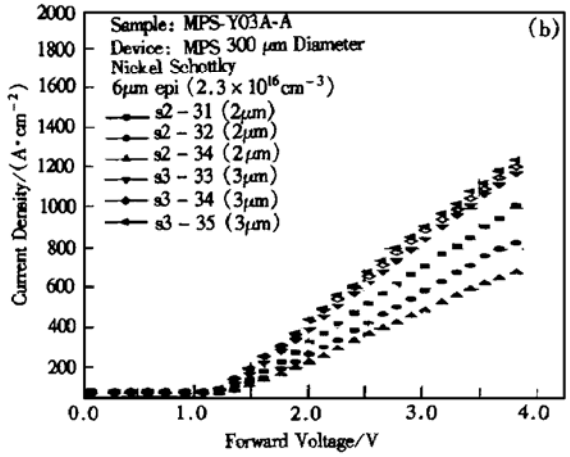

FIg. 4(b) Forward Characteristics of MPS Diode with 300μm Diameter and Ni Contact

From the forward I-V characteristics, the turn-on voltage of the 4H-SiC MPS diodes with Ni contact can be seen about 1.25V. The level-off of the forward current at a high forward bias is caused by the series resistance of diodes. The forward current density of MPS diode is a little higher if the reverse leakage current density is higher. Figure 4(b) shows the forward I-V characteristics of some 4H-SiC MPS devices with diameter of 300μm and different Schottky contact ring width (ranging between 2μm and 3μm). Obviously, higher forward current density can be obtained with a smaller width of the junction implantation window. The dead space below the junction is minimized at the place where the current does not flow. For 3μm devices, the forward current density is higher than 1000A/cm^2 at 3.5V (on-state resistance R_{on}= 3.5mΩ·cm^2) while it is higher than 600A/cm^2 for 2μm devices. Why small devices have high forward current density is not clear at this moment.

4 Summary and Conclusion

4H-SiC MPS diodes with Ni Schottky contact and junction termination extension (JTE) edge termination have been successfully designed, fabricated and characterized. The devices can block more than 600V reverse voltage, which is about 70% of the parallel plane junction breakdown voltage, and the lowest leakage current at - 600V is 1×10^{-3}A/cm^2, while the forward current density at 3V is more than 200 A/cm^2 for 1000μm devices, 1000A/cm^2 at 3.5V for 300μm devices. It shows that the reverse characteristics of the reverse leakage current are determined by the screening effect of the p-n junctions. It demonstrates that lower barrier Schottky metal can be used for MPS diode fabrication, with which, lower turn-on voltage can be obtained, while our keeping the low reverse leakage current. Further efforts are needed to optimize the fabrication in order to get a lower reverse leakage and higher forward conduction.

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4H-SiC 混合 PN/Schottky 二极管的研制

张玉明[1] 张义门[1] P. Alexandrov[2] J. H. Zhao[2]

(1 西安电子科技大学微电子所, 西安 710071, 中国)

(2 Department of Electrical and Computer Engineering, The State University of New Jersey, NJ 08854-8058, USA)

摘要: 报道了 4H-SiC 混合 PN/Schottky 二极管的设计、制备和特性. 该器件用镍作为肖特基接触金属, 使用了结终端扩展 (JTE) 技术. 在肖特基接触下的 n 型漂移区采用多能量注入的方法形成 P 区而组成面对面的 PN 结, 这些 PN 结将肖特基接触屏蔽在高场之外, 离子注入的退化是在 1500℃下进行了 30min. 器件可耐压 600V, 在 600V 时的最小反向漏电流为 1×10^{-3}A/cm^2. 1000μm 的大器件在正向电压为 3V 时电流密度为 200A/cm^2, 而 300μm 的小尺寸器件在正向电压为 3.5V 电流密度可达 1000A/cm^2.

关键词: 功率器件; 碳化硅; 半导体二极管; MPS

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张玉明 男, 1965 年出生, 博士, 副教授, 从事新型半导体器件、TCAD 和 VLSI CAD 的教学和科研工作. 目前主要研究碳化硅器件的器件物理、工艺、模型和模拟.

张义门 男, 1941 年出生, 教授, 博士导师, 主要从事 VLSI 中器件的模型和模拟、VLSI CAD、量子阱器件和宽禁带高温微电子学.

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