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# SILC Mechanism in Degraded Gate Oxide of Different Thickness

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**Abstract**: It is shown that traps are generated asymmetrically in the thin gate oxides with different thickness during high field degradation, as well as the multi-mechanism plays role in the Stress Induced Leakage Current (SILC). These factors perform differently in gate oxide of different thickness. A comparison is drew between several analyzing models. Trap assisted tunneling is preferred for thinner samples, while Pool-Frankel like mechanism or thermal emission mechanism should apply to the thick ones.

**Key words**: SILC; gate oxide
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## 1 Introduction

SILC is the phenomenon of abnormal increase in low field gate current in the stressed gate oxide. SILC current $I_{SILC}$ can be defined as $I_{SILC} = I(t) - I(0)$, in which $I(t)$ is the gate current at the stress time $t$, and $I(0)$ is the gate current of a new device. SILC, occurring before the device breakdown, has had harmful influence upon the reliability of thin gate MOSFETs. Owing to the generation of the traps during the degradation, SILC can cause the degradation of data retention in the flash memory device. Though the origin of SILC has been reported for several times[1—5], still no full understanding has been reached. Several models have been employed to analyze the SILC[1,6—8], among which, trap assisted tunneling model, thermal assisted tunneling and resonant tunneling model are the most popular. In this paper, the comparison between the experimental results on thin gate oxide of 4, 5, 7 and 9nm samples shows that the trap distribution can not be regarded as uniform positive charged traps or neutral traps merely. Multi current mechanism exists in SILC for samples of different thickness.

## 2 Experiment

Samples were 4, 5, 7 and 9nm nMOSFET's with $W/L$ being 15μm/15μm. Using HP4156, different constant voltages were applied as both positive and negative bias. After each cycle of stress, the gate current-voltage characteristics were measured as well as the subthreshold gate voltage variation $\Delta V_g$. The experimental results were recorded automatically by computer.

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## 3 Results and Discussion

Figure 1 is the $I_g$–$V_g$ curve, which shows the different performance of samples having different thickness. For 4nm and 5nm samples, the SILC phenomenon appears in the low field, while the current at high voltage almost keeps constant. For 7nm sample, SILC also appears in the low field, but at high field the current decreases, with a cross point existing at about 6V. For 9nm sample, no SILC can be observed. There are two kinds of opinions, one is that SILC is caused by the neutral trap[6], while the other is that the SILC is caused by positive charges in the oxide[9].

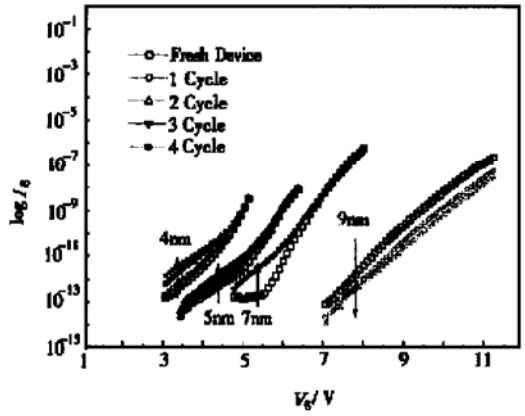


FIG. 1 nMOSFET log$I_g$–$V_g$ curve for Samples of Different Thickness Before and After Stress The low field currents of 4nm, 5nm, and 7nm show obvious increase.

Though the gate current increases in the low field and almost keeps unchanged in the high one for 4nm and 5nm samples, the subthreshold gate voltage (shown in Figure 2) however, continually increases, as means the net charge in the oxide is negative. It seems that along with more negative charges existing in the oxide, more positive charges will be close to the anode or the conduction band of $SiO_2$.

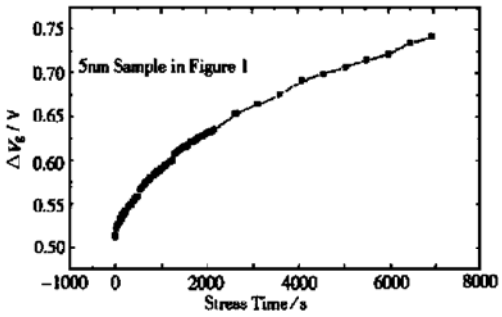


FIG. 2 Variation in Subthreshold Voltage After Longtime Stress for the 5nm Sample in Figure 1

Figure 3(a) shows the formation of such a distribution: the trapped negative charges (electrons) near the anode or in the shallow traps can tunnel out of the traps easily, while positive charges are

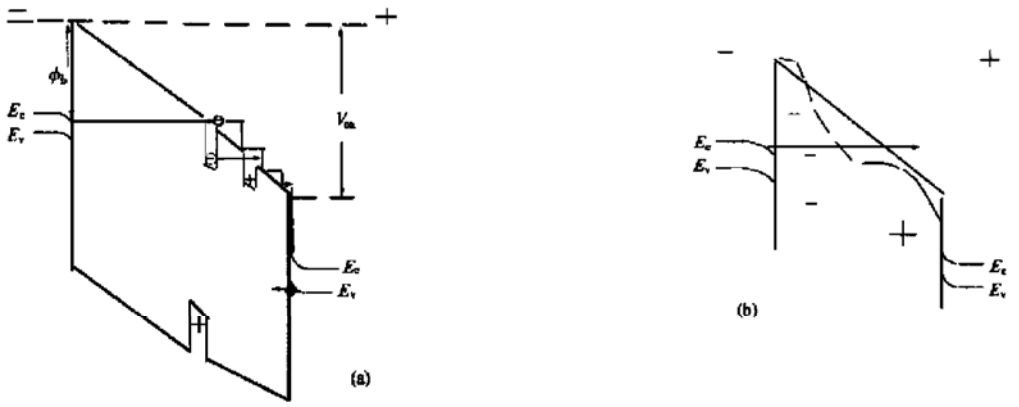


FIG. 3 (a) Trapped electron can easily tunnel out of the trap while the hole is left in the trap; (b) Barrier increases near the cathode and lowers near the anode. Solid curve: fresh device barrier. Dashed line: barrier after long-time degradation.

more inclined to be left in the traps. Moreover, the hole mobility in oxide is much smaller than that of the electron. Therefore, the electrons can tunnel much longer than holes, no matter how the holes are injected into the oxide, i. e., the shallow traps and those near the anode will be positively charged or remain neutral, while the traps near the cathode are negatively charged by injected electrons. Due to such an asymmetrical distribution, the $SiO_2$ barrier becomes a complicated-shaped one, as is shown in Figure 3(b). The barrier near the cathode increases while the one near the anode falls.

Both the positive and negative $I_g$-$V_g$ measurements after the stress cycle show similar increase in low field current, which are considered symmetric. The traps are also deduced to be uniformly distributed across the oxide. In fact, after long-time stressing, the positive and negative characteristics are different. In the positive bias measurement, low field current increases continually as a decreasing function of the measuring voltage until breakdown, while in the negative bias measurement, it increases as an increasing function of the voltage, as is clearly shown by $J(t)/J(0)$-$V_g$ plot in Figure 4 and may be caused by the increase of positively charged traps near the anode. $J(t)$ is the gate current density after the stress time $t$; $J(0)$ is that of fresh device. Anode hole injection has also been reported[9], though its mechanism has not been very clear. No impact ionization can occur in the thin oxide, owing to the trap generation. There exist many complex bond structures on the interface of cathode and anode, some of which can be easily broken below 2eV, the source of holes back injected[4]. The injection distance and energy distribution depend on the injection field and the oxide thickness. Some evidence also shows the trap distribution to be nonuniform[10,11].

For thin samples, such as 4nm and 5nm ones, the barrier near the cathode is almost 'apparent' for the electrons from the cathode, so more electrons have a 'direct' tunneling from the cathode to the conduction band. For thick samples, at a voltage within the range of measurement, one electron injected from the cathode must tunnel a distance that is longer than one free path (about 2.7nm)[12]. At high voltages, electrons will be scattered because of the increased barrier near the conduction band, in this way, a FN like course occurs; at low voltages, a trap assisted tunneling is preferred and SILC appears.

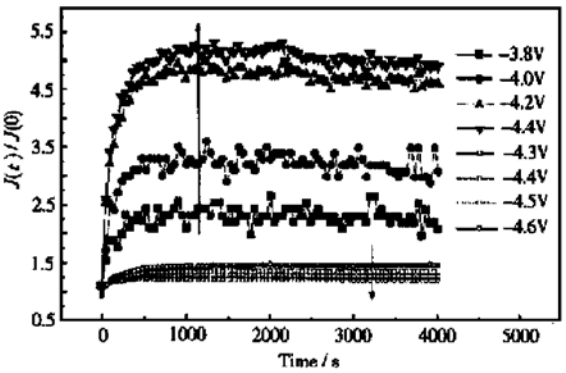


FIG. 4 $J(t)/J(0)$: time character of a degraded 5nm sample by different positive and negative measurement. $J(t)$ is the gate current density after stress time $t$ and $J(0)$ is that before degradation.

No SILC can be observed in 9nm samples, which does not imply that no SILC exists in thicker samples. Most likely, it is due to the tiny current within the measuring voltage range. Anyway, the SILC phenomenon in thicker oxides has been proved by using a special method[8].

Pool-Frankel model and Schottky like emission model have been presented on the assumption of positive trap[13], both of which have a linear relation with the squareroot $E_{ox}$ and a change in the conduction barrier height. From the linear fitness in Figure 1, it can be seen that in 4nm and 5nm samples, the slope changes little after stress, i. e. the change in barrier height is little, so the above two models are inaccurate. The mechanism is also denied by the 1/f noise measurement[14]. For thin oxides, both the deep traps near the anode and the shallow ones have the possibility of assisting the tunnel electrons injected from the cathode. It can be easily explained by the model of Chou and Lai[15]. For thicker oxides, however, the SILC

mechanism is complicated. Several mechanisms work together, with the possibility of thermal emission. From Fig. 1, we can see that the barrier height changes obviously after stress for 7nm sample.

The performance of 4nm sample and 5nm sample is quite different. In Fig. 1, the best linear fitness is seen for 5nm sample, which indicates a single mechanism is dominant; 4nm sample has a little deviation from the linear relation, which is because of the increase of interface traps. Interface trap can make the anode barrier lower and induce the recombination current on the interface. In samples less than 3.5nm, it is proved that the $I_{SILC}$ is mainly due to interface traps. The interface trap induced current can be neglected[16] in the low field for thicker samples[17].

## 4 Conclusion

The gate current can be expressed as $I_g = I_{FN} + I_{SILC}$, where $I_{SILC}$ includes two components. $I_{ot}$ is part of the oxide trap effect. $I_{it}$ is part of the interface effect that can be neglected in the low field in thick oxides. The mechanism of $I_{ot}$ is different for samples of different thickness. For thicker oxides, several mechanisms may work together, while for thinner ones, trap assisted tunneling is a better explanation. The trap distribution in oxide is nonuniform. For samples thinner than 4nm, the effect of interface trap becomes more serious.

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# MOSFET 不同厚度薄栅老化中 SILC 的机制


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**摘要**：通过对栅电流和栅电压漂移的测量，证明了均匀 FN 应力老化后栅氧化层中陷阱呈非均匀分布．不同厚度的栅氧化层产生 SILC 的机制不尽相同，薄栅以陷阱辅助隧穿为主，类 Pool-Frankel 机制在厚二氧化硅栅中起主导作用．



**关键词**：应力感应漏电；栅氧化层

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