第 22 卷第 4 期　　半 导 体 学 报　　Vol. 22, No. 4
2001 年 4 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Apr., 2001

Resistivity Instability in Polysilicon Resistors Under Metal Interconnects and Its Suppression by Compensating Ion Implantation

YU Ning-mei, GAO Yong and CHEN Zhi-ming

(*School of Automation & Information Engineering, Xi'an University of Technology, Xi'an 710048, China*)

Abstract: The resistivity instability of the boron-doped polysilicon resistors being a line resistance element of ICs is within the range of several kΩ's, especially when our running the underneath metal interconnects. Polysilicon resistors have been fabricated under various processing conditions as well as some electrical and crystallographic characteristics have been obtained. It is shown the resistivity instability mainly results from the variational carrier mobility. By analyzing the Seto's model, the barrier height and trapped charge density are observed reducing under the Al over layer. Therefore, the resistance instability is also caused by both the charge trapping/detrapping occurring at polysilicon grain boundaries and the resultant variation in the potential barrier height. The formation of high-stability polysilicon resistors in the range of several kΩ's has been decided by compensating the ion implantation, which makes the charge trapping/detrapping at the grain boundary less susceptible to the hydrogen annealing.

Key words: polysilicon; interconnect
PACC: 7280C; 7360J　　**EEACC**: 2520; 2550
CLC number: TN43　　**Document code**: A　　**Article ID**: 0253-4177(2001)04-0511-05

1 Introduction

A line resistance element is an integrant part of analog integrated circuits, which also plays an important role in the very large scale digital integrated circuits, including SRAM cell, PROM's, ECL and different types of logic circuits. Polysilicon resistors apply to above usage because of some of its characteristics, such as parasitic capacitance, no substrate-bias dependence, significantly reducing the die area and excellent compatibility with the existing device processing modules[1—3]. However, it is known that the resistance of polysilicon changesdrastically in the doping range of 10^{18}—10^{19} cm^{-3}, while it is quite difficult to obtain a stable resistance value in the range of several kΩ's. The resistivity instability becomes more striking when our running the underneath metal interconnects. In order to develop high performance LSI, the wring of gate area is demanded to be arbitrary and the polysilicon resistance to be as stable as possible. Therefore, it is very important to stabilize the polysilicon resistance and adjust the resistor values in IC's after fabrication[4]. In this paper, a peculiar phenomenon of resistivity instability is introduced for the first time, which occurs only in polysilicon huge resistors when we are running the underneath

YU Ning-mei was born in 1962. She gained Doctor's degree from North East University in Japan in 1998. Her current research interests focus on the high speed ICs design and the processing technologies.

GAO Yong was born in 1956. He is currently a professor in the Department of Electronics Engineering of Xi'an University of Technology. His research interests are in the novel power semiconductor device, ICs CAD and integrated opto-electronics.

CHEN Zhi-ming was born in 1945. He is currently a professor in the Department of Electronics Engineering of Xi'an University of Technology. His research interests are in the SiC materials, novel power device and power IC.

Received 21 February 2000, revised manuscript received 15 August 2000

aluminum interconnects. It is demonstrated that such instability can be well suppressed by compensating the ion implantation. For a better understanding of the phenomenon, the polysilicon resistors have been fabricated under various processing conditions, at the same time, the electrical and the crystallographic characteristics are also concluded. As a matter of fact, the charge trapping/detrapping at polysilicon grain boundaries and the resultant variation in the potential barrier height will result in the resistivity instability. It is also shown that the acceptor/donor compensating doping can stabilize the grain-boundary charge, thus the instability is suppressed.

2 Experimental Procedures

The polysilicon resistors were fabricated according to the following procedures: First, 100nm-thick SiO_2 was thermally grown on p-type(100) silicon wafers. Then, 300nm-thick polysilicon films were deposited on the thermal oxide by low-pressure chemical-vapor deposition (LPCVD) of SiH_4 pyrolysis in N_2 atmosphere at 550℃ and annealed at 1100℃ for 1h for grain growth. Then the films were doped by implantation, which was followed by the post-implantation that had been annealed at 1150℃ for 20s. After the 300nm-thick CVD SiO_2 was deposited, Al electrode was formed and PSG was deposited. Finally, a layer of aluminum was deposited. The resistivity was measured in the structure, with or without an Al overlayer, as is shown in Fig. 1. For the samples without the Al overlayer, the aluminum was etched immediately after the Al deposition, while for those with the Al overlayer, it had to be annealed at 450℃ for 30min.

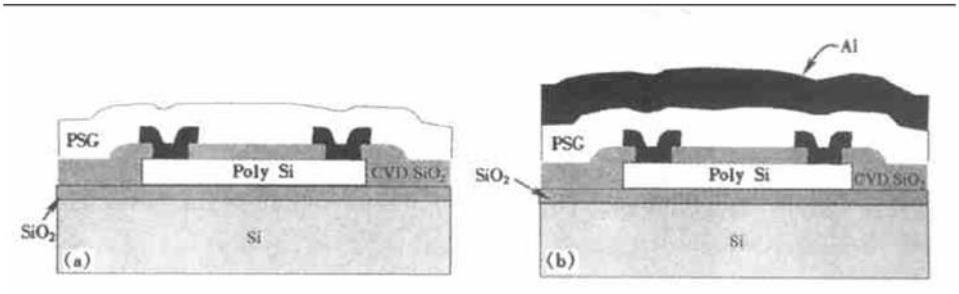

FIG. 1 Structures of Polysilicon Resistors (a) Without and (b) with Aluminum Interconnect Running over Poly Resistor

3 Experimental Results

The variations in the polysilicon resistor with a boron dose of $1\times10^{14}cm^{-2}$ are shown in Fig. 2 as a function of the annealing temperature. The samples were annealed in N_2 atmosphere for 30min. More than a factor of two difference is seen between the samples with and without an Al overlayer at temperatures above 430℃(typical post-metallization annealing temperature). It is seen that the polysilicon resistance is influenced by Al wiring.

It is well known that the resistance of polysilicon is related to the grain size, Hall mobility, carrier concentration and other factors. In order to find out the cause of resistivity instability in polysilicon resistors under metal interconnects, all the poly film resistivity, Hall mobility, carrier concentration and grain size are observed. Fig. 3(a) and (b) demonstrate the TEM photomicrographs of 1×10^{14} cm^{-2} boron implanted polysilicon films with and without Al overlayer. An average grain size measured from TME is 0.127μm. No remarkable difference is observed between two types of samples. Therefore, the carrier deactivation within the grains is expected to be the reason for the resistance difference. The boron-dose dependence of poly film resistivity, Hall mobility and carrier con-

centrations are shown in Table 1. Under the same implantation condition, it is noted that though the carrier concentrations are the same, there exists great difference in the mobility between two samples.

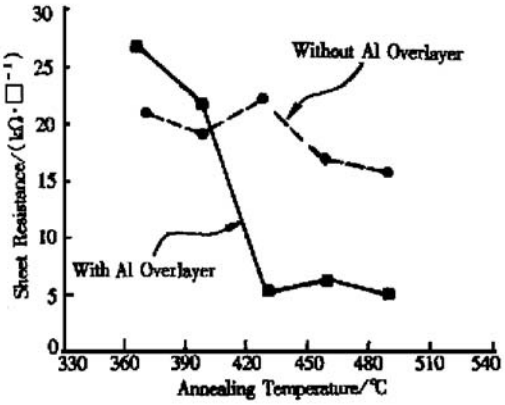

FIG. 2 Sheet Resistance of Polysilicon Resistor Implanted with $1\times10^{14}cm^{-2}$ of Boron as Function of Post-Metallization Annealing Temperature

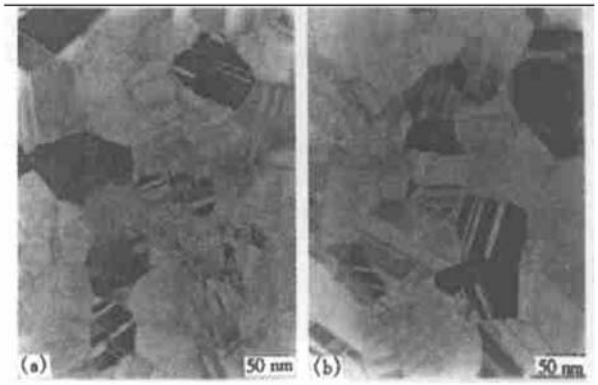

FIG. 3 TEM Photomicrographs of $1\times10^{14}cm^{-2}$ Boron Implanted Polysilicon Films (a) with and (b) Without Al Overlayer

Table 1 Resistivity, Carrier Density, Hall Mobility, Barrier Height and Trapped Charge of Different Samples

Boron Dose/cm^{-2}	Al	Resistivity /(Ω·cm)	Carrier Density /$10^{18}cm^{-3}$	Hall Mobility /($cm^2\cdot V^{-1}\cdot s^{-1}$)	Barrier Height /eV	Trapped Charge Density/$10^{12}cm^{-2}$
1.0×10^{14}	without	0.2070	3.06	9.91	0.0808	3.61
	with	0.1070	3.03	10.94	0.0539	2.93
3.0×10^{14}	without	0.0299	10.7	19.60	0.0386	4.66
	with	0.0224	11.3	24.70	0.0249	3.84
6.0×10^{14}	without	0.0112	23.2	24.00	0.0250	5.52
	with	0.0108	23.4	24.90	0.0170	4.57

In order to investigate the reason for the difference in mobility, the temperature dependence of resistivity has been measured and the height of the potential barrier on the grain boundaries obtained. According to Seto's model[5], the height of the potential barrier on the grain boundary E_B is expressed as

$$\sigma = 1/\rho = Lq^2p(1/2\pi m\times kT)^{1/2}\exp(-qV_B/kT) \quad (1)$$

where L is the grain size, p is the carrier concentration.

So,

$$\rho \propto T^{1/2}\exp(qV_B)/kT) \quad (2)$$

$$E_B = qV_B \quad (3)$$

And

$$V_B = qQ_t^2/8\epsilon p \quad (4)$$

where Q_t is the trapped charge density.

The barrier height and the trapped change density can be calculated from the temperature characteristic of resistivity and Eqs. (3) and (4), as shown in Table 1. Obviously, they are both reduced under the Al overlayer, which might be due to the increase of mobility under the Al overlayer.

Therefore, the resistivity instability in boron-doped polysilicon high resistors has been observed in the range of several kΩ's when our running the underneath metal interconnects. In order to improve the situation, the technology of boron/phosphorus compensating the ion implantation has been developed in this paper. The dotted lines in Fig. 4 denote that the sheet resistance of the polysilicon samples versus the single boron dose after annealing at 450℃. The solid curves show the results after compensating implantation where the abscissa

represents the net acceptor dose that is compensated by the background donor (phosphorus) doping of $5\times10^{14}cm^{-2}$ at 75keV. In the case of compensating implantation, the boron dose of the cross axis shows excessive boron dose. There is much difference between the samples with and without Al overlayer under the single boron implanted condition. In contrast, the sheet resistance of these two samples is similar for the purpose of compensating implantation. The resistivity instability occurred underneath the Al overlayer can be suppressed by the compensation ion implantation.

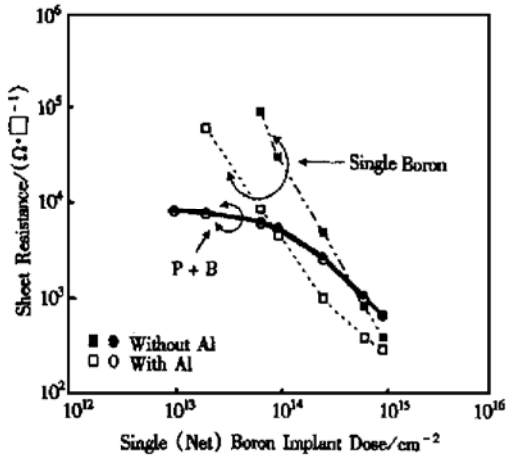

FIG. 4 Sheet Resistance of Polysilicon Resistor After 450℃ Post-Metallization Annealing as Function of Net Acceptor (Boron) Dose

4 Discussion

We tentatively interpret the phenomena in terms of the enhanced hydrogen annealing effect occurring in the presence of aluminum. Presumably, the OH groups and/or H_2O molecules adsorbed on the surface of CVD SiO_2 would be reduced by the Al, with hydrogen released to passivate the boundary traps. The grain boundaries of both boron and phosphorus (or arsenic) implanted polysilicon have proved very stable against hydrogen annealing. Impurity segregation at the grain boundary may change the chemical structure of the boundary but the details are not known at present.

5 Conclusion

In conclusion, the formation of high-stability polysilicon resistors in the range of several kΩ's has been established by compensating the ion implantation, which makes the charge trapping/detrapping at the grain boundary less susceptible to the hydrogen annealing.

References

[1] Nicky Chau-chun Lu, L. Gerzberg *et al.*, IEEE Trans. Electron Devices, 1982, **29**(4): 682—690.

[2] A. Kalnisky, Jia Li and C. E. Daniel Chen, IEEE Trans. Electron Devices, 1993, **40**(2): 358—363.

[3] D. W. Lee, T. M. Roh *et al.*, Electron. Lett., 1999, **35**(7): 603—604.

[4] D. W. Felbaumer, J. A. Babcock *et al.*, IEEE Trans. Electron Devices, 1995, **42**(4): 689—696.

[5] J. Y. W. Seto, J. Appl. Phys., 1975, **46**(12): 5247—5254.

集成电路中金属连线下多晶硅电阻的不稳定性分析及抑制方法

余宁梅　高　勇　陈治明

(西安理工大学 自动化与信息工程学院，西安　710048)

摘要：作为集成电路的电阻单元，掺硼的多晶硅电阻在千欧级的范围内存在阻值不稳定性，尤其在金属连线下更为严重. 分析了不同工艺条件下制作的多晶硅电阻电特性和晶格特性. 结果表明，阻值的不稳定性主要由载流子迁移率改变引起. 通过测试和运用 Seto's 模型计算进一步发现，在铝连线底下势垒高度和俘获的电荷密度均有降低. 电荷的俘获/反俘获在多晶硅晶粒边界发生引起势垒高度的变化，从而导致阻值不稳定. 然后，借助于补偿的离子注入制作了高稳定的、阻值在千欧级的多晶硅电阻. 该方法使得多晶硅晶粒边界电荷的俘获/反俘获对氢退火不敏感.

关键词：多晶硅；互连

PACC：7280C；7360J　　EEACC：2520；2550

中图分类号：TN43　　**文献标识码**：A　　**文章编号**：0253-4177(2001)04-0511-05

余宁梅　女，1962 年出生，博士，主要研究方向为高速 IC 设计及工艺技术.

高　勇　男，1956 年出生，教授，主要研究方向为新型功率半导体器件、IC 设计和集成光电子.

陈治明　男，1945 年出生，教授，主要研究方向为 SiC 材料、新型功率器件和功率 IC.

2000-02-21 收到，2000-08-15 定稿