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A Novel Sub-50nm Poly-Si Gate Patterning Technology*

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Abstract: A novel low-cost sub-50nm poly-Si gate patterning technology is proposed and experimentally demonstrated. The technology is resolution-independent, i.e., it does not contain any critical photolithographic steps. The nano-scale masking pattern for gate formation is formed according to the image transfer of an edge-defined spacer. Experimental results reveal that the resultant gate length, about 75 to 85 percent of the thickness, is determined by the thickness of the film to form the spacer. From SEM photograph, the cross-section of the poly-Si gate is seen to be an inverted-trapezoid, which is useful to reduce the gate resistance.

Key words: poly-Si gate; sub-50nm; image transfer; lithography
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1 Introduction

Feature size of MOS devices has been scaled down into sub-100nm regime after the development for more than two decades, aiming at obtaining higher packing density, faster circuit speed and lower power dissipation[1]. However, the traditional optical photolithographic technique leaves a lot to be desired in bringing MOS devices into the sub-100nm regime, though it is progressing rapidly in recent years[2]. Gate patterning is one of the most important technologies in the sub-100nm generation. High-resolution patterning of critical features for sub-100nm devices is investigated by using X-ray lithography[3], electron beam lithography[4], extreme ultraviolet (EUV) lithography[5], etc. However, it cannot be put into practice very soon because of a lot of unsolved technical problems and the requirements of the complicated and high-cost equipment. Simple and low-cost patterning techniques for sub-100nm devices have attracted much attention. Photoresist ashing technique proposed by Chung[6] is a low-cost method, but owing to the additional electron beam lithographic step during the sub-100nm gate fabrication[7], it is difficult to have the resist-ashing process under good control.

In this paper, a novel resolution-independent lithographic sub-50nm gate patterning technique, called edge-defined patterning, is proposed, with which 40nm poly-Si gates have been fabricated successfully. Experimental results show that it can offer excellent uniformity and controllability.

2 Experiments

Schematic cross-sections of the major fabrication processes of sub-50nm poly-Si gate line are

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shown in Fig. 1. The starting substrate is 100mm P-type silicon wafer with ρ being 10—20Ω·cm. After the thermal growth of a 5nm gate oxide, 200nm gate poly-Si, 50nm buffer nitride and again 200nm sacrificial poly-Si were deposited orderly by LPCVD as shown in Fig. 1(a). Then, a conventional lithographic step was done with the sacrificial poly-Si film etched to form sidewalls, seen in Fig. 1(b). After the deposition of 50nm oxide by LPCVD, it was etched by reactive ion etch (RIE). As a result, the oxide spacers were formed against the sidewalls of the sacrificial poly-Si layer, seen in Fig. 1(c). The residual sacrificial poly-Si layer was subsequently moved into the KOH solution. After that, all the buffer nitride films except for those masked by oxide spacers were etched by RIE, as is shown in Fig. 1(d). The oxide spacers were then moved into the BOE solution. Consequently, as is shown in Fig. 1(e), the rectangle nitride caps were formed to mask the gate poly-Si. At last, the poly-Si film was etched by RIE and the nitride caps were moved into hot H_3PO_4, seen in Fig. 1(f). Obviously, no critical photolithographic step is needed, that is to say, the technology is resolution-independent.

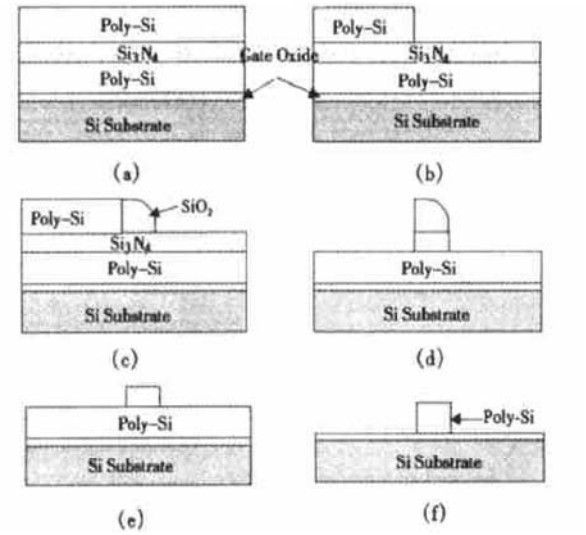

FIG. 1 Schematic Cross-Sections of Major Fabrication Processes of Sub-50nm Poly-Si Gate

For the sake of comparison, the technology proposed by Horstmann[8] *et al.*, with a major procedure being shown in Fig. 2, was also demonstrated according to above steps, where the oxide was used as the sacrificial layer and the nitride as the material to form the spacers, was used directly as the masking layer in the poly-Si gate formation.

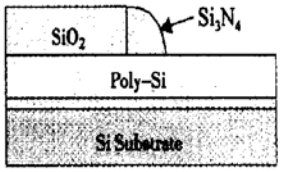

FIG. 2 Schematic Cross-Section of Major Procedure During Fabrication in Reference[8]

3 Discutions and Results

Figure 3 shows a SEM photograph of the cross-section of a 40nm poly-Si gate line fabricated in this experiment. SEM measurement reveals that the lengths of the poly-Si gate lines are about 75 to 85 percent of the thickness of the oxide to form spacers. And, the lengths depend upon the thickness of the oxide, if only the sacrificial poly-Si is

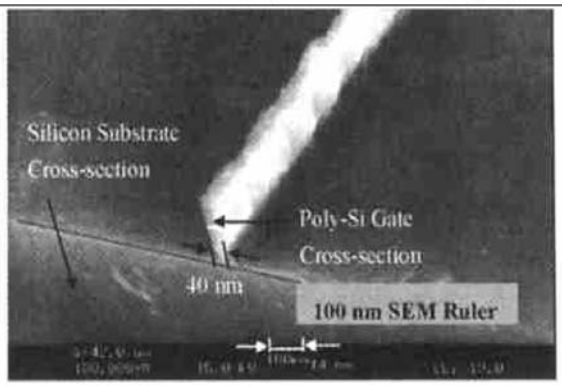

FIG. 3 SEM Photograph of Cross-Section of a 40nm Poly-Si Gate Fabricated by Using Technology Proposed in This Work

twice as thick as that of the oxide at least. In this way, excellent uniformity and controllability of gate length can be obtained. The smallest thickness of the oxide used in this work is 50nm. So, the poly-Si gates with length shorter than 40nm are expected to be obtained by using this method if the thickness of the oxide is thinner than 50nm. Seen in Fig. 2, the cross-section of the gate is in the shape

of inverted-trapezoid. The inverted-trapezoid gate has lower resistance than the trapeziform or rectangular one, because at the same gate length and thickness, inverted-trapezoid has larger cross-sectional area. Therefore, the novel edge-defined gate patterning technology is more suitable for the sub-100nm generation applications.

Figure 4 shows a SEM photograph of the cross-section of a 150nm poly-Si gate line fabricated with the technology proposed in Reference[8], which is seen to be an irregular polygon, as is consistent with the results reported in Reference[8]. This can be attributed to the triangular-alike nitride mask for gate patterning. In this letter, the mask for gate patterning is a regular rectangle. Hereby, the novel gate patterning technology is more preferable.

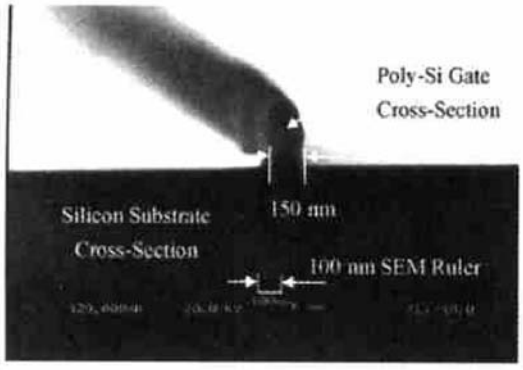

FIG. 4 SEM Photograph of Cross-ection of a 150nm Poly-Si Gate Fabricated by Using the Process in Reference[8]

4 Conclusions

A novel edge-defined poly-Si gate patterning technology is proposed, which is low-cost and resolution-independent. Poly-Si gates with the length of 40nm have been successfully fabricated by using this technology. It is believed that the poly-Si gates with length shorter than 40nm can also be obtained if the thickness of the spacer film can be reduced further. Moreover, the novel technology potentially provides the Poly-Si gates with low gate resistance, compared with the conventional technologies. All of above makes the technology attractive in the sub-100nm MOS device and nanoelectronics applications.

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新型亚 50 纳米硅栅制作技术*

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摘要: 提出并演示了一新型的低成本亚 50 纳米多晶硅栅制作技术. 该技术的特点是它与光刻分辨率无关, 即不需要高分辨率光刻技术. 纳米尺度的栅掩膜图案是由台阶侧壁图形的转移所形成. 实验结果表明, 该技术制成的硅栅的栅长由形成侧壁图形的薄膜之厚度所决定, 大致为该厚度的 75%—85%. SEM 照片显示硅栅的剖面为倒梯形结构. 与其它结构 (如矩形或正梯形) 相比, 该结构有利于减少栅电阻.

关键词: 硅栅; 亚 50nm; 图形转移; 光刻

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