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A Radiation Hardened Power Device——VDMNOSFET

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Abstract: A radiation hardened N-channel Si power device——VDMNOSFET (Vertical Double-Diffused Metal Nitride-Oxide Semiconductor Field Effect Transistor) is fabricated by using a double layer (Si_3N_4-SiO_2) gate dielectric and a self-aligned heavily doped shallow P^+ region. The effects of ionizing radiation and transient high dose rate radiation of the power VDMNOSFET are also presented. Good radiation hardening performance is obtained, compared with the conventional power VDMOSFET. For the specified 200V VDMNOSFET, the threshold voltage shifts is only − 0.5V at a Gamma dose of 1Mrad (Si) with + 10V gate bias; the transconductance is degraded by 10% at a Gamma dose of 1Mrad (Si); and no burnout failures occur at the transient high dose rate of 1×10^{12}rad (Si) /s. It is demonstrated that the ionizing radiation tolerance and burnout susceptibilities of the power MOSFET are improved significantly by using a double layer (Si_3N_4-SiO_2) gate dielectric and a self-aligned heavily doped shallow P^+ region.

Key words: radiation hardening; double layer gate dielectric; power VDMNOSFET
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1 Introduction

The advanced power VDMOSFETs have been widely used in solid state power systems because of its inherent advantages. But its characteristics are degraded in the radiation environment, such as space radiation, nuclear power stations, etc. The effects of radiation on power VDMOSFETs have been investigated during the last decades[1]. The main failure modes are the negative shift in threshold voltage and the degradation in transconductance with ionizing radiation, due to the accumulation of positive charge, and the increase of interface states at the Si/SiO_2 interfac, respectively. Transient high dose rate radiation may result in a power VDMOSFET burnout.

In previous method, the radiation tolerance of MOSFET is improved by reducing the gate oxide thickness[2]. However, a very thin gate SiO_2 layer has a poor resistibility to the H^+ ions drift and H_2 diffusion toward the Si-SiO_2 interface, so it is easy to break down. H^+ ions and H_2 diffusion are the main reasons for the generation of the positive charges and latent interface-trap after irradiation[3]. Therefore, a very thin gate SiO_2 layer is unsuitable for the high voltage radiation hardened power VDMOSFET.

The burnout susceptibility of N-channel power MOSFET has been investigated by Keshavarz

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et al. with simulation methods[4] based on the conventional VDMOSFET structure. The results indicate that significant improvement in radiation tolerance and burnout of the device is attributed to the reduce in the lateral size of the power MOSFET's cell or the lowered emitter inject-efficiency of the bipolar structure. But conventional radiation hardened VDMOSFET structure can not satisfy the requirements effectively.

In this paper, we reported a kind of radiation hardened power device—— VDMNOSFET, manufactured with a double layer (Si_3N_4-SiO_2) gate dielectric and a self-aligned heavily doped shallow P^+ region.

2 Device Structure

In order to enhance the radiation tolerance of VDMOSFET, gate dielectric and device structure should be improved. Radiation-induced charges in the gate oxide and the interface state generation at the Si-SiO_2 interface are the main cause of the shift in threshold voltage and degradation in transconductance. The threshold voltage shift can be expressed as[5]

$$|\Delta V_T| = \frac{q}{C_{ox}T_{ox}}\int_0^{T_{ox}} xp(x)\,dx \qquad (1)$$

where C_{ox} is the gate oxide capacitance per unit area, T_{ox} is the gate oxide thickness, $p(x)$ is the radiation-induced charge density distribution in the gate oxide layer. Equation (1) can be expressed as:

$$|\Delta V_T| = \frac{q}{\epsilon_{SiO_2}\epsilon_0}\int_0^{T_{ox}} xp(x)\,dx \qquad (2)$$

The radiation-induced interface state density, ΔN_{it}, decreases the carrier mobility in the inversion layer, which can be expressed as[6]

$$\mu = \frac{\mu_0}{1 + \alpha\Delta N_{it}} \qquad (3)$$

where μ_0 and μ are the pre-and post-irradiation carrier mobilities in the channel, respectively; α is a constant.

Consequently, the decrease in the carrier mobility after radiation exposure degrades the transconductance of the device. From Eq. (3), we obtain:

$$G_m = \frac{G_{mo}}{1 + \alpha\Delta N_{it}} \qquad (4)$$

where G_{mo} and G_m are the pre- and post-irradiation transconductance, respectively. From Eqs. (2) and (4), it is found in order to decrease ΔV_T and improve G_m, the trapped charge and interface state density should be reduced as much as possible. In addition, ΔV_T is decreased by increasing ϵ_{SiO_2}, i. e. it is beffer to replace SiO_2 by another dielectric. The trapped charges and the interface state density are related to both the oxide film and the oxide processes. According to the model proposed by Sah[7], the gate oxide process should be under careful control and the SiO_2 thickness should be reduced, which are necessary for the fabrication of high quality SiO_2 films and Si-SiO_2 interface. However, because of the existence of hydrogen in the poly-Si gate and CVD oxide, H^+ ions drift and H_2 diffusion toward the Si-SiO_2 interface are the main origin of positive charge and latent interface-trap generation after irradiation[3]. With poor resistibility to H^+ ions drift and H_2 diffusion toward the Si-SiO_2 interface, the single very thin gate oxide layer is easy to break down.

Therefore, double layer (Si_3N_4-SiO_2) gate dielectric films have been developed to improve the ionizing radiation tolerance of high voltage power VDMOSFETs. The Si_3N_4-SiO_2 structure has many advantages. Because holes are more mobile than electrons in chemically vapor deposited (CVD) Si_3N_4[8], there are a number of electron traps in CVD Si_3N_4 and the increase in the interface state density is very small after ionizing radiation exposure for Si_3N_4-SiO_2[9]. Moreover, Si_3N_4 films are of higher dielectric constant, higher breakdown strength and higher resistibility to H^+ ions drift and H_2 diffusion toward the Si-SiO_2 interface, so the susceptibility to radiation is reduced, compared with SiO_2 films. In this paper, the gate dielectric thickness is 100nm, which is composed of 30nm SiO_2 grown at 1000℃ in high purity dry O_2 and

70nm Si_3N_4 deposited by LPCVD.

The burnout appears due to the existence of parasitic NPN transistor, shown in Fig. 1. Conventional VDMOSFETs have a deficiency, namely the deep diffused P^+ junction. Alignment errors can cause nonuniformity in the P-base resistance and lead to nonuniform current conduction in the interior of the device. In addition, owing to the deep diffused P^+ region, the device scaling is limited; the cell-packing density is reduced and a higher on-resistance is obtained. The P^+ inner concentration is low because of the deep diffusion. The parasitic BJT is most likely to turn on due to the large lateral current flow in the p-base region, as is obvious when the device is exposed to the transient high dose rate irradiation. It is the cause of the power VDMOSFET burnout. Recently, a new VDMOSFET structure has been reported based on a super self-aligned process technology[10], which integrates a heavily doped shallow self-aligned P^+ region under the source N^+ region to reduce the p-base sheet resistance, as is shown in Fig. 2. This new structure has many advantages, such as dramatic reduction in the parasitic BJT current gain and p-base sheet resistance, low on-resistance, high cell packing density. Moreover, the current is confined vertically from the drain to the source rather than flowing laterally through the p-base region when the device breaks down due to impact ionization[11]. This is an effective way to suppress the turn on of parasitic BJT and eliminate the thermal breakdown. Fortunately, these characteristics are identical with the simulation results of Keshavarz[4] to improve the radiation burn out susceptibility of N-channel power MOSFETs.

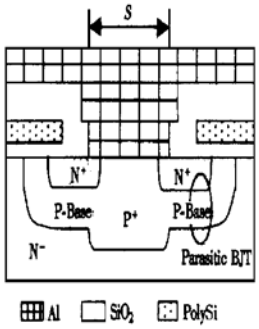

FIG. 1 Schematic Illustration of Conventional VDMOSFET Structure

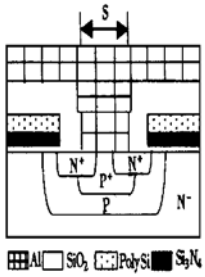

FIG. 2 Schematic Illustration of Radiation Hardened VDMNOSFET Structure

In summary, the radiation hardened power VDMNOSFET has the Si_3N_4-SiO_2 gate dielectric and with a self-aligned heavily doped shallow P^+ region, as shown in Fig. 2.

3 Results and Discussion

Two batches of transistors have been fabricated. One is VDMOSFET with conventional structure, the other is VDMNOSFET. The starting materials are < 100 > orientation, N/N^+ epitaxial wafers. A poly-Si gate is selected since it can provide good passivation for the gate dielectric against the ingress of mobile ions. The poly-Si thickness is 600nm. The N^+, P and P^+ regions are formed by As^+ and B^+ ions implantation with the dose of 5×10^{15}, 4×10^{13} and $5\times10^{15}\,cm^{-2}$, respectively. Their junction depth is 0.5, 3 and 2μm, respectively, as shown in Fig. 2. The deep P^+ region in Fig. 1 is formed by diffusion with 5μm junction depth. Both batches of chips are packaged in TO-220 package. Devices with limits of 200V and 5A have been made. The transconductance of devices is 1S when V_{DS}= 20V, V_{GS}= 5V. The threshold voltage V_T is 3.5V when I_{GS}= 1mA.

Gamma total dose irradiation experiment has

been performed, with the devices exposed when V_{GS} = + 10V and the dose rate being 200krad(Si)/h. The threshold voltage, V_T at which I_D= 1mA, is defined as the gate voltage. The threshold voltage shifts, ΔV_T, versus Gamma total dose without applied bias and with a bias V_{GS} of + 10V are shown in Figs. 3 and 4, respectively. The variety in transconductance versus the Gamma total dose is shown in Fig. 5. The effect of ionizing radiation on the I_D–V_{GS} relationship for VDMNOSFET is shown in Fig. 6.

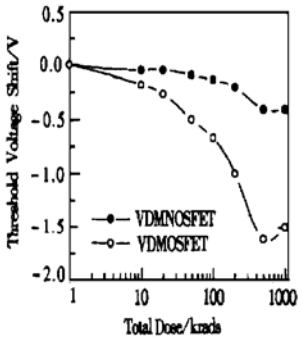

FIG. 3 Threshold Voltage Shift vs Total Dose at V_{GS}= V_{DS}= 0V

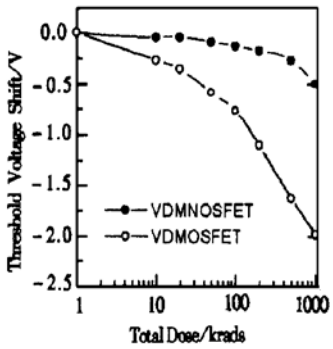

FIG. 4 Threshold Voltage Shift vs Total Dose at V_{GS}= 10V, V_{DS}= 0V

The threshold voltage of the conventional VDMOSFET has fallen by – 1.7V at 500krad(Si), but rises remarkably at 1Mkrads, as can be seen in Fig. 3, which is not obvious in VDMNOSFET. The shift in threshold voltage is only – 0.5V for VDMNOSFET but – 2V for VDMOSFET when V_{GS}= + 10V at 1Mrad(Si), as shown in Fig. 4. The transconductance is degraded by only 10% for VDMNOSFET but 50% for VDMOSFET at 1Mrad(Si) as is shown in Fig. 5. It indicates that a large number of interface states have been induced during the high dose irradiation in conventional VDMOSFET, while it is not so serious in VDMNOSFET. It can also be demonstrated by the degradation of transconductance, as is shown in Fig. 5.

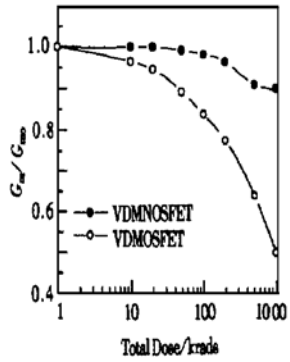

FIG. 5 Change of Transconductance vs Total Dose

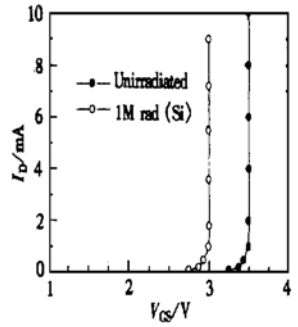

FIG. 6 Effect of Ionizing Radiation on I_D–V_{GS} Relationship for VDMNOSFET

In order to examine the devices susceptibility to transient high dose rate irradiation, the devices are exposed to Gamma dose rates of 1×10^{11} rad(Si)/s and 1×10^{12} rad(Si)/s, respectively. It is indicated that all VDMOSFETs fail at 1×10^{11} rad(Si)/s when the bias V_{DS}= 140V. Burnout has been observed. But in VDMNOSFETs, no burnout failures have been observed even at the dose rate of 1×10^{12} rad(Si)/s when the bias V_{DS}= 140V. The VDMNOSFETs exhibit a very good radiation burnout resistance, due to the self-aligned heavily doped shallow P^+ region, which can overcome the disadvantages of conventional power VDMOS–

FET.

Experimental results also prove the simulation results of Keshavarz[4] and the self-aligned heavily doped shallow P^+ region structure proposed by Shenai[11] effective in improving the high dose rate transient irradiation tolerance of power VDMOSFET.

4 Conclusion

We have developed a radiation hardened power VDMNOSFET. It is demonstrated that the ionizing radiation tolerance and burnout susceptibilities of power MOSFET can be improved significantly by using a double layer Si_3N_4-SiO_2 gate dielectric and a self heavily doped shallow P^+ region. Devices with useful electrical and radiation-hardening characteristics have been put into practice.

References

[1] T. P. Ma and P. V. Dressendorfer, Ionizing Radiation Effects in MOS Devices and Circuits, New York: Wiley, 1989.

[2] G. B. Roper and R. Lowis, IEEE Trans. Nucl. Sci., 1983, **NS-30**(6): 4110.

[3] A. Jaksić *et al.*, 1997 Fourth European Conference on Radiation and its Effects on Components and Systems Proceedings, Palm Beach, Cannes, France, 1997, 36—42.

[4] A. A. Keshavarz *et al.*, IEEE Trans. Nucl. Sci., 1992, **NS-39**(6): 1943.

[5] D. L. Blackburn *et al.*, IEEE Trans. Nucl. Sci., 1983, **NS-30**(6): 4116.

[6] K. F. Galloway *et al.*, IEEE Trans. Nucl. Sci., 1986, **NS-33**(6): 1454.

[7] C. T. Sah, IEEE Trans. Nucl. Sci., 1976, **NS-23**(6): 1563.

[8] B. H. Yun, Appl. Phys. Lett., 1975, **27**(4): 256.

[9] K. Watanabe *et al.*, IEEE Trans. Nucl. Sci., 1986, **NS-33**(6): 1216.

[10] K. Shenai, IEEE Trans. Electron Devices, 1992, **ED-39**(5): 1252.

[11] K. Fischer *et al.*, IEEE Trans. Electron Devices, 1996, **ED-43**(6): 1007.

一种抗辐射加固功率器件——VDMNOSFET

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摘要：采用 Si_3N_4-SiO_2 双层栅介质及自对准重掺杂浅结 P^+ 区研制出了一种抗辐射加固功率器件——VDMNOSFET (垂直双扩散金属-氮化物-氧化物-半导体场效应晶体管). 给出了该器件的电离辐射效应及瞬态大剂量辐射的实验数据，与常规 VDMOSFET 相比获得了良好的抗辐射性能. 对研制的 200V VDMNOSFET，在栅偏压+ 10V，γ 总剂量为 1Mrad (Si) 时，其阈值电压仅漂移了- 0.5V，跨导下降了 10%. 在 γ 瞬态剂量率达 1×10^{12}rad (Si) /s 时，器件未发生烧毁失效. 实验结果证明 Si_3N_4-SiO_2 双层栅介质及自对准重掺杂浅结 P^+ 区显著地改善了功率 MOS 器件的抗电离辐射及抗辐射烧毁能力.

关键词：抗辐射加固；双层栅介质；功率 VDMNOSFET

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