第 22 卷第 8 期　　半 导 体 学 报　　Vol. 22, No. 8
2001 年 8 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Aug., 2001

Forward Gated-Diode Monitoring of F-N Stressing-Induced Interface Traps of NMOSFET/SOI*

HE Jin, HUANG Ai-hua, ZHANG Xing and HUANG Ru

(*Institute of Microelectronics, Peking University, Beijing* 100871, *China*)

Abstract: The forward gated-diode R-G current method is used to monitor the F-N stressing-induced interface traps of NMOSFET/SOI. This simple and accurate experiment method can directly give the interface trap density induced by F-N stressing effect for characterizing the device's reliability. For the measured NMOS/SOI device with a body structure, an expected power-law relationship as $\Delta N_{it} \sim t^{0.4}$ between the pure F-N stressing-induced interface trap density and the accumulated stressing time is obtained.

Key words: F-N effect; stressing-induced interface trap density; R-G current; gated-diode; MOSFET/SOI
EEACC: 2560R; 2530; 1570D
CLC number: TN386　　**Document code**: A　　**Article ID**: 0253-4177(2001)08-0957-05

1 Introduction

It is well known that as the transistor dimension shrinks to the sub-micron and deep sub-mic-ron range, strong lateral and normal electrical fields lead to many new effects, which induce interface traps and bulk traps adjacent to the drain and channel regions. These induced traps seriously degrade the performance and reliability of the MOSFET's. In order to control the transistor performance, it is essential to accurately monitor the interface traps induced by the variation of the effects.

Applying stressing to MOSFET device is one of the methods widely used in determining the change of stressing-induced Si/SiO_2 interface trap density and hot carrier effect of the MOSFET. In the past decades, various experiment methods have been employed to exam the magnitude of stressing-induced interface trap, such as I-V, I-t, C-V or charge-pumping measurements[1,2]. However, when device geometry goes much smaller, the signal error due to the increasing parasitic effect makes such measurements insensitive, inaccurate, and more complex.

Recently, a refined gated-diode structure has often been used to characterize the interface traps and extract the bulk carrier recombination lifetime in the SOI device by measuring the recombination-generation (R-G) current, some very good results have been achieved[3—6]. It has been shown that the method is simple, sensitive, quickly applicable and nondestructive.

In this paper, we demonstrate the validity of the forward gated-diode R-G current method to characterize the average interface trap density induced by the F-N stressing for SOI NMOSFET.

* Project Supported by Motorola CPTTL (Contract No: MSPSDDLCHINA-0004).

HE Jin male, post-doctoral researcher. His current research interests focus on the deep sub-micro SOI device optimum and characterization and new MOS-based power devices.

ZHANG Xing professor. He has been working in the area of sub-micro CMOS/SOI process, simulation and design of ASICs since 1986.

Received 22 December 2000, revised manuscript received 3 March 2001

This method is applied to an NMOSFET/SOI with a body contact structure. Through scanning the gate voltage, the forward current in the diode formed between source/drain and body regions shows a sharp current peak, which is responsible for the channel interface traps induced by the strong field F-N stressing. The measurement results show that the average interface trap density induced by the F-N stressing increases in a power law of a factor 0.4 with the accumulated stressing time.

2 Structure and Measurement

The cross-section of a SOI lateral gated-diode used in the R-G current measurement is shown in Fig. 1. If we apply a small (< 0.6V) forward bias to this diode, the total diode current includes the diffusion current as well as the recombination-generation current due to the front and back silicon/silicon oxide interface traps. By scanning the front or/and back gate voltage, the interface traps can be activated or otherwise screened. As a result, the diode current will demonstrate a strong R-G current peak when the interface is in the depletion state. The magnitude of the peak value directly reflects the interface trap density.

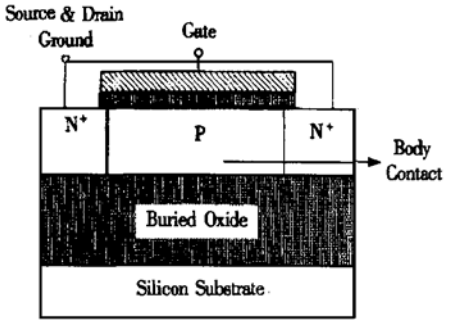

FIG. 1 Cross-Section of Gated-Diode Structure Used in Measurement

In our studied NMOS/SOI device, this method is realized with a body contact structure, as shown in Fig 1. The gated-diode consists of the source and drain/body N^+ P^- junction. The measured NMOSFET/ SOI was fabricated on the SIMOX wafer with a 20μm channel width and 10μm channel length. The gate oxide thickness (t_{ox}), the buried oxide thickness (t_{box}) and the silicon film thickness (t_{Si}) are respectively 16, 360 and 190nm.

In the measurement, the source and drain contacts are connected to ground while applying a bias of 0.45V to body contact. As a result, between the source/drain and the body regions forms a forward p-n junction diode. By scanning the gate voltage, we can obtain the measured forward R-G current. We apply a constant stress on the gate to perform F-N stressing conditions, i. e., a gate voltage of 3V while the source and body contacts are grounded. The accumulated stressing time was changed from 10s, through 20s, 50s, 80s, 100s, 200s, 500s, 800s, 1000s, to 2000s. The measurement conditions are chosen as follow: the body bias voltage is 0.45V while the source and drain contacts are grounded to form the forward diode. Through scanning the front gate voltage from -1V to 4V, the measured current will contain the contribution from the R-G of the interface traps generated by the F-N stres-sing.

3 Results and Discussion

In the weakly forward bias mode (operating in the sub-threshold region of the diode), the body contact current comprises the small diode diffusion current and the R-G current at the Si-SiO_2 interface traps. Maximum recombination at the interface traps occurs when the intrinsic Fermi level is at the midway between the electron and the hole quasi-Fermi levels or N_s-P_s. Scanning the gate voltage to vary the silicon surface from accumulation to depletion state, the maximum recombination condition is satisfied along the channel from the source junction toward the drain junction. And then the presence of the interface traps localized in the channel region of the increased interface would be manifested by an R-G current peak, as shown in Fig. 2 where the total body contact current increases exponentially with the forward bias

voltage magnitude as predicted by the SRH theory.

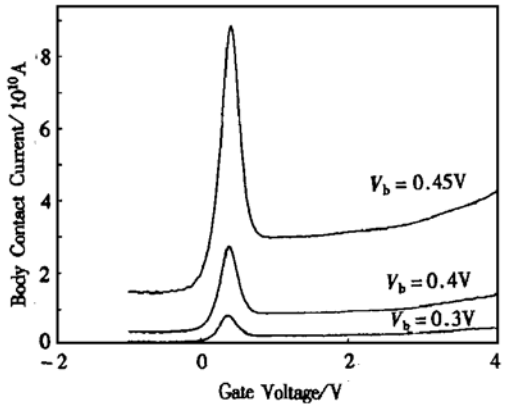

FIG. 2　Source/Drain-Body Diode Current as a Function of Gate Voltage for Different Forward Bias Voltages Under the Condition Without F-N Stressing

Based on the above mentioned principle, the F-N stressing induced interface trap will contribute a pure part of the R-G current, leading to the R-G current peak in the gate bias scanning curve to rise. Therefore, the increased amplitude of the R-G current peak could be used in determining the F-N stressing induced pure interface trap density. The following measurement and the calculation are just based on this discussion.

Figure 3 plots body contact current against gate bias, showing the evolution of the R-G current with the F-N stressed time. Following the stressing, a current peak is observed, attributed to the increase in the interface trap recombination. The peak current grows in magnitude, exhibiting a strongly time dependence. Based on these measurements, the pure increased R-G current induced by the F-N effect can be simply modeled by the following formula for different stressing times.

$$\Delta I_{\text{pure}} = I_{\text{stress, j}} - I_{\text{without stress}} \qquad (1)$$

Thus, the extracted pure increased R-G current peak values for different F-N stressing times are shown in Fig. 4.

Based on SRH statistics theory, the relationship between pure increased R-G current peak va-lue and interface trap density can be

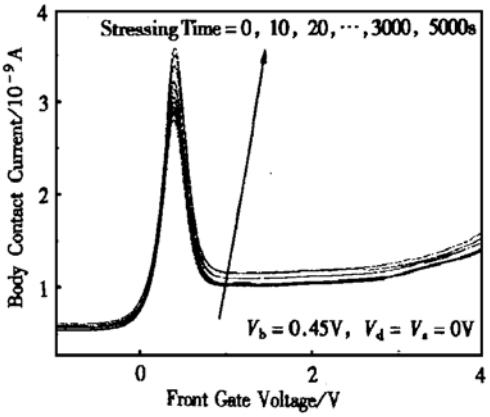

FIG. 3　Source/Drain-Body Diode Current as a Function of Gate Voltage for Different Accumulated Stressing Times

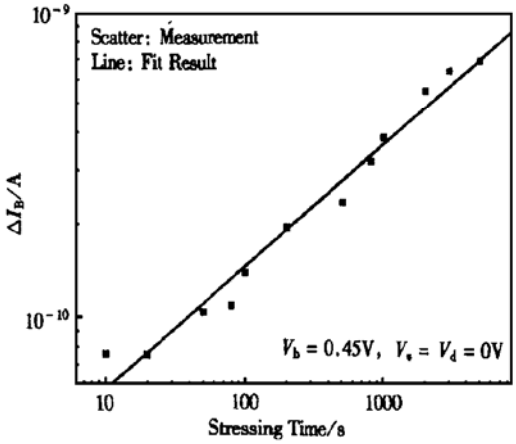

FIG. 4　Measurement of Pure Stressing-Induced R-G Current Value as a Function of Accumulated Stressing Time

described simply by:

$$\Delta I_{\text{pure}} = \frac{1}{2} q n_i (c_n c_p)^{1/2} N_{it} A_G e^{\frac{qV_b}{2kT}} \qquad (2)$$

where n_i is intrinsic carrier density, N_{it} is the density of interface traps, A_G is gate area, and V_b is the small forward-voltage we apply to the diode. Here, $c_n = c_p = 10^{-8}\text{cm}^{-3} \cdot \text{s}^{-1}$[3].

From Fig. 4, we can obtain the R-G current peak values for each measurement at first. And then, using equation (2), we can easily calculate the corresponding density of the interface trap density (N_{it}) after stressing. Finally, by subtracting the original interface trap density, we can find the relationship between stressing-induced

interface trap density and accumulated stressing time. For a given MOS/SOI, a group of similar measurements using this method can be performed, and the corresponding factor n can be calculated, as shown in Fig. 5.

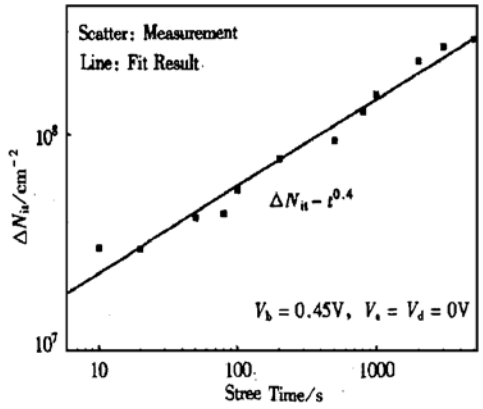

FIG. 5 Measurement and Fit Result of Pure Stressing-Induced Average Interface Trap Density as a Function of Accumulated Stressing Time

As shown in this figure, the interface trap density grows in magnitude, exhibiting logarithmic time dependence. From this plot, we can further reveal that the pure F-N stressing-induced interface trap density increases in a power law with the relationship of $\Delta N_{it} \sim t^n$, here factor n is fitted to be 0.4. This result is consistent with the earlier observation[7]. Apparently, the smaller the factor n, the better the stressing character of this device, and the longer the operating lifetime of it (MOS/SOI device).

4 Conclusion

We have investigated the forward gated-diode R-G current measurement of the silicon/silicon oxide interface trap induced by the F-N stressing in an NMOS/SOI device in this paper. By applying this method to the NMOSFET/SOI with a body contact structure, expected power law relationship as $\Delta N_{it} \sim t^{0.4}$ between the pure F-N stressing-induced interface trap density and the accumulated stressing time has been obtained.

Acknowledgements The authors would like to thank Dr. Wang Hong-mei for her providing experiment samples and Dr. Zhang Yao-hui, and Mr. Mark Foisy from Motorola for their helps.

References

[1] A. Pacelli, A. L. Lacaita and S. Villa, Reliable Extraction of MOS Interface Traps from Low Frequency *CV* Measurements, IEEE Electron Device Lett., 1998, **19**: 148—150.

[2] C. H. Ling, S. E. Tan and D. S. Ang, A Study of Hot Carrier Degradation on NMOSFET's by Gate Capacitance and Charge Pumping Current, IEEE Trans. Electron Devices, 1995, **42**: 1321—1328.

[3] Xue Jun Zhao and Dimitris E. Ioannou, A Sensitive Tool for Characterizing the Buried Si-SiO_2 Interface, Proceeding of 1999 IEEE International SOI Conference, Oct., 1999, 52—53.

[4] T. Ernst, S. Cristoloveau, A. Vandooren *et al.*, Recombination Current Modeling and Carrier Lifetime Extraction in Dual-Gated Fully-Depleted SOI Devices, IEEE Trans. Electron Devices, 1999, **46**: 1503—1509.

[5] He Jin, Huang Ru, Zhang Xing *et al.*, Numerical Analysis of Characterizing Back Interface Traps of SOI Devices by R-G Current, Chinese Journal of Semiconductors, 2000, **21**(12): 1146—1151.

[6] He Jin, Zhang Xing, Huang Ru *et al.*, Dependence of R-G Current of the Forward Gated-Diode on Bulk Trap Characteristics and Silicon Film Structure Parameters, Chinese Journal of Semiconductors, 2001, **22**(1): 18—24.

[7] Chen Ming-hu, Simon. C. Tam, Fu. Chen Hsu, Ping-Kenung Ko, Tung-Yichan and Kylew W. Terrill, Hot-Electron-Induced MOSFET Degradation Model, Monitor and Improvement, IEEE Trans. Electron Devices, 1985, **32**: 375—385.

正向栅控二极管监测 F-N 电应力诱生的 SOI-MOSFET 界面陷阱*

何　进　黄爱华　张　兴　黄　如

(北京大学微电子学研究所，北京　100871)

摘要: 报道了正向栅控二极管 R-G 电流法表征 F-N 电应力诱生的 SOI-MOSFET 界面陷阱的实验及其结果. 通过体接触的方式实现了实验要求的 SOI-MOSFET 栅控二极管结构. 对于逐渐上升的累积应力时间, 测量的栅控二极管电流显示出明显增加的 R-G 电流峰值. 根据 SRH 理论的相关公式, 抽取出来的诱生界面陷阱密度是随累积应力时间的上升而呈幂指数的方式增加, 指数为 0.4. 这一实验结果与文献先前报道的基本一致.

关键词: F-N 应力效应; 界面陷阱; R-G 电流; 栅控二极管; MOSFET/SOI.

EEACC: 2560R; 2530; 1570D

中图分类号: TN386　　**文献标识码**: A　　**文章编号**: 0253-4177(2001)08-0957-05

* Motorola 和北京大学联合资助项目(合同号: MSPSDDLCHINA-0004).

何　进　男, 33 岁, 博士后. 目前研究方向为深亚微米 MOS 器件、功率 MOS 器件、深亚微米 MOS 新结构的设计和表征等.

张　兴　男, 35 岁, 教授, 博士导师. 研究方向为深亚微米 MOS 器件、工艺和 ASIC 设计.

2000-12-22 收到, 2001-03-03 定稿