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Design of 1GHz Local Oscillator with DLL-Based Frequency Multiplier Technique

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Abstract: A new method of synthesizing 1GHz based on a 0.5μm CMOS DLL is proposed, which can synthesize frequency with simple logic and amplifiers. The designed frequency synthesizer consists of a DLL (Delay-Locked Loop) and a building block of synthesizing logic. The reference frequency input into this frequency synthesizer is 25MHz and the synthesized frequency is 1GHz.

Key words: DLL; PLL; frequency synthesizer; VCDL; VCO; transceiver; local oscillator
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1 Introduction

One of the key building blocks associated with a receiver or transmitter is a frequency generating or synthesizing device that can create a Local Oscillator (LO) signal to shift down (downconvert) a received carrier signal spectrum to a lower frequency, or in a transmitter, to shift the signal spectrum up to a higher frequency band. The LO is traditionally implemented by using a Phased-Locked Loop (PLL) synthesizer, with a Voltage Controlled Oscillator (VCO) as the frequency generating device. In a fully integrated synthesizer, the VCO is a limiting factor due to the over phase noise performance. In this paper, a synthesizer based on DLL is considered as an alternative, in which, the frequency-generating device is replaced by a Voltage Controlled Delay-Line (VCDL) having inherent lower phase noise. The phase noise of the VCDL-based synthesizer is limited by a crystal oscillator, which is of much better inherent phase noise performance than the VCO[1].

The DLL-based frequency multiplier consists of a DLL and a synthesizing logic, illustrated in Fig. 1, with an 80-delay-stage as an example. Accepting the low-frequency crystal oscillator input, the DLL generates the multiple delayed edges. In case the loop is in a locked condition, ref and sla are still in-phase. Evenly spaced within one period of the crystal frequency, the DLL output edges can form the higher-frequency transitions. The synthesizing logic takes each edge from the DLL, and then an output frequency $40f_{ref}$ is generated.

A VCDL can produce multiple delayed phases of a high Q crystal input signal (25MHz in this design). In this synthesizer, many edges are attempted to be combined into a single output waveform. The edge combining circuitry, namely synthesizing logic, is the most critical component in this design. The design has a tradeoff between the power consumption and phase noise. One edge

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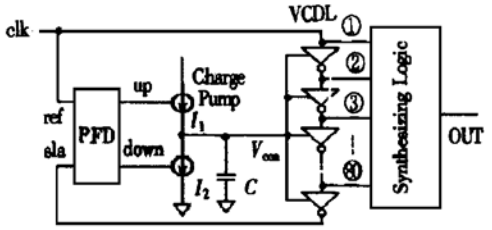

FIG. 1 Diagram of the Frequency Synthesizer Based on DLL

combining circuitry with a 900MHz output frequency described in Reference[2] is shown in Fig. 2, where the differential input ports produced by using the VCDL in a DLL, 1P1N, 2P2N, 3P3N, …, 9P9N, are triggered in turn by the evenly spaced edges, whose differential outputs, loaded by respective LC-tanks, are all connected to OUT+ and OUT−. This topology, however, to the differential inverter units in Fig. 2, complementing the function of wire-or, finally creates a multiplied signal. A high jitter performance is offered at the expense of a large DC current consumption by the differential units. A new approach to the evenly spaced edges combination by using VCDL in a DLL and making full use of the merits of a DLL is described below, with less power dissipation and excellent jitter performance obtained.

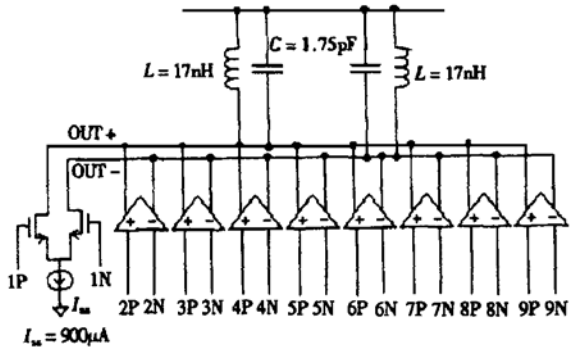

FIG. 2 Circuit Schematics for Edge Combiner

Now let's describe how this DLL-based frequency synthesizer works. In a stable state, the delay of the VCDL in the DLL is just one period of the input signal, T_{clk}. In this design, given a factor of 40, the VCDL is evenly divided so that 80 identical delaying units are obtained, each of which is an inverter, whose delay is controlled by the voltage. Thus, the waves of the inverters' outputs are obtained and shown in Fig. 3 (for the sake of convenience, only 8 points are offered). It can be seen that after being delayed by $T_{clk}/80$ and inverted, the next wave is produced. Combining (1) AND(2), (3) AND(4), (5) AND(6), (7) AND(8), we can synthesize the frequency. The wave at point of out is the output we want.

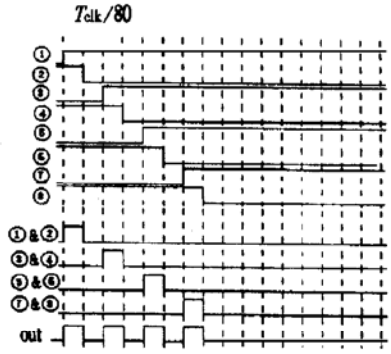

FIG. 3 Waves of the Delay Units (8 Points)

With a VCO, the problem of vibrating is unavoidable in a PLL. Further more, since one pole is offered by the VCO and the other by the charge pump, a PLL is at least a 2nd order system. It is difficult to solve a problem involving a 2nd PLL. For example, if you want to reduce the time needed to lock the PLL, a relatively small capacitor in the charge pump is necessary. However, this capacitor in the Charge Pump can not be too small for fear that there be a large jitter in the PLL. On the other hand, if you want to get a small jitter, a big capacitor must be used in the charge pump, as, however, makes the system take a long time to reach the stable state. Fortunately, no such a problem is involved in a DLL, because owing to the replacement of the VCO in PLL by a VCDL in DLL, which does not offer a pole to the system, the DLL belongs to a 1st order system. Theoretically, 1st system is stable and it is easier to make a tradeoff in a DLL than that in a PLL. The capacitor in the charge pump of a DLL can be as small as possible and the jitter in a DLL do not vary as much as that in a PLL.

2 Synthesizing Logic

Figure 4 is the diagram of the block of the synthesizing logic. The points 1—80 in this figure are the counterparts in the VCDL. As described above, the narrow pulse of the a1—a40 at the outputs of the AND gates are of the same period but not the same phase, and the difference in phase between one and its next is the same. Should all the narrow pulses be overlaid, we can get the multiplied frequency. But it is difficult to add all the narrow pulses by logic only because we can not make an OR gate having 40 inputs. A lot of methods have been tried for the added output but fail to work well. The amplitudes we get are not high enough, and the symmetry has also been destroyed. An improved approach is shown in Figure 4. The NMOS M1—M40, as well as the R_1, can sum up 40 narrow pulses, which are known as wire-or. Because the pulses are too narrow ($T_{clk}/80$ is equal to 500ps), the summed signal is too small in amplitude, and its operating point is not $V_{cc}/2$ at point b, either. With the capacitor C, we insulate the DC and a resistor(R_2) biased inverter to get the operating point $V_{cc}/2$. The inverter used here can also offer some voltage gains, behind which, there are other two inverters to be used to buffer the output. The input frequency used in this design is 25MHz; the output frequency is 1GHz; the synthesizing factor is 40.

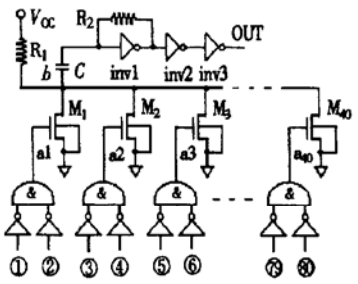

FIG. 4　Synthesizing Logic

In Fig. 4, R_1 and R_2 introduce DC currents. The voltage of the point b fluctuates around the certain DC voltage, owing to its failure to fully charge or discharge quickly enough the charges stored in the capacitance related to the point b; R_2 biases inv1 in Fig. 4 to $V_{cc}/2$, as makes the DC current through inv1. It is reasonable to trade off carefully in the choices of R_1 and R_2 to get the as small power dissipation as possible.

3 Simulation Results by HSPICE

The simulation conditions:

Power Supply	3V
Temperature	25℃
Process	DPDM 0.5μm CMOS
Model	BSIM2
Foundry	TSMC
Software	HSPICE

Figure 5 shows the simulation results. CLK is the input(25MHz), out is the final output(1GHz), which is previously 40 times as much as the input frequency. The V_{con} in this figure is the controlling voltage of the VCDL. From the V_{con}, we find that the transient time is less than 2μs. Because it has no difficulty in tradeoffs, it is easy to reduce the transient time or further enhance the stability. The V_{con} is an exponential, which is one of the characteristics of 1st order system.

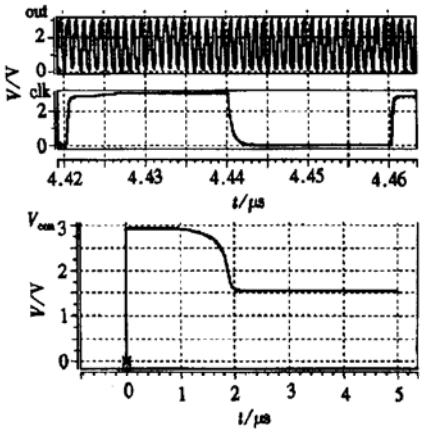

FIG. 5　Simulation Results of the Design

4 Conclusions

DLL-based frequency multipliers have a

fundamentally different phase noise signature compared with PLL-based ones. In a PLL, the output timing uncertainty accumulates many oscillation cycles, which is limited by the time response of the PLL[5]. As for a DLL-based frequency multiplier, each output edge only contains the timing uncertainty accumulated in the previous delay stages within the same crystal period. Therefore, the limited jitter accumulation translates into a flat phase noise profile with less offset frequencies than the reference. As a result, long-term error accumulation, or the close-in phase noise, is much lower than that in a typical VCO.

It is very difficult to realize a frequency synthesizer with a DLL, especially when the synthesized frequencies are at RF bands. The method described in this paper has proved reasonable to synthesize the frequency by simple logic and amplifiers. By taking the advantage of the characteristics of DLLs, many high quality RF frequency synthesizers can be obtained, so it is a new approach to implement all the RF functions in a single chip with CMOS technology only[6]. It is also an alternative to implement a DDFS to synthesize the frequencies without ROM[7].

References

[1] George Chien, Monolithic CMOS Frequency Synthesizer for Cellular Applications, http: // buffy. eecs. berkeley. edu/IRO/Summary/98 abstracts/gchien. 1. html.

[2] George Chien and Paul R. Gray, A 900-MHz Local Oscillator Using a DLL-Based Frequency Multiplier Technique for PCS Applications, http: // kabuki. eecs. berkeley. edu/~ gchien/papers/isscc00/isscc2kdigest. PDF.

[3] R. E. Best, Phase-Locked Loops, Second Edition, New York: McGraw-Hill, 1993.

[4] W. F. Egan, Frequency Synthesis by Phase Lock, New York: Wiley & Sons, 1981.

[5] L. Lin, L. Tee and P. R. Gray., A 1.4GHz Differential Low-Noise CMOS Frequency Synthesizer Using a Wideband PLL Architecture, in Digest of Technical Papers, IEEE International Solid-State Circuit Conference, 2000, 204—205.

[6] A. Abidi *et al.*, The Future of CMOS Wireless Transceivers, Digest of Technical Papers, International Solid-State Circuit Conference, 1997, 118—119.

[7] A. Rofougaran, G. Chang, J. J. Real, J. Y.-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M.-K. Ku, E. W. Roth, A. A. Abidi and H. Samueli, A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS—Part Ⅰ: Architecture and Transmitter Design, IEEE J. Solid-State Circuits, 1998, **33**(4): 515—534.

基于 DLL 倍频技术的 1GHz 本地振荡器设计

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摘要: 介绍了一种基于 0.5μm CMOS DLL 合成 1GHz 信号的新方法. 这种方法的特点是只通过使用简单的逻辑和放大来产生倍频信号. 该设计的频率合成器包括两个部分: 一个 DLL (Delay-Locked Loop) 和一个频率合成逻辑模块. 输入的参考频率是 25MHz, 合成的输出频率为 1GHz.

关键词: 延时锁相环; 锁相环; 频率合成器; 压控延时线; 压控振荡器; 收发器; 本地振荡器

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