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High Performance VHF Power VDMOSFETs for Low Voltage Applications

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Abstract: A high performance VHF power VDMOSFET, applying to the mobile communications, is developed, which can deliver an output power of 12W with the drain efficiency of 70% as well as the gain of 12dB at a low supply voltage of 12V and 175MHz. It is fabricated by using the terraced gate structure and refractory molybdenum (Mo) gate technology.

Key words: low voltage; terraced gate structure; Mo gate technology; VHF power VDMOSFET
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1 Introduction

It is well known that the demand for high frequency high power silicon VDMOSFETs that apply to HF, VHF, and UHF band is increasing, because of their advanced inherent characteristics, such as fast switching response, excellent thermal stability, large safe operating area, high input impedance and simple control-circuit configuration.

Usually, higher supply voltage (28V or 50V) and higher power are applied in the RF field. However, in the application of mobile transmitters, FM broadcast transmitters, military communication transmitters, AM aircraft transmitters and base stations, low voltage operations are required with high efficiency and high gains, i. e. a device with small capacitance, low on-resistance and high frequency is necessary.

High performance and high frequency power VDMOSFETs, which can operate at a low supply voltage (e. g. 12V) at VHF band, have been rarely reported at present. The device has a low cut-off frequency at the low voltage that is primarily caused by the large gate-drain capacitance, C_{GD}. Acting as the Miller capacitance[1,2], C_{GD} results from the thin gate oxide and a relatively high gate resistance R_G of the self-aligned polysilicon process. To meet the high frequency specifications, both C_{GD} and R_G should be reduced. Although some VDMOSFETs structures have been proposed to reduce C_{GD} effectively[2,3], there are some limitations, such as the increase of R_{ON}[3] and the decrease of breakdown voltage[4].

In this paper, a high performance high

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frequency power VDMOSFET is reported by using a terraced gate structure and refractory Mo gate technology to reduce C_{GD} and R_G.

2 Device Design and Structures

In order to realize the high frequency and high power operation at a low voltage, we gave some assumptions of the output power and high frequency performance.

2.1 Output Power P_O

The output power, P_O, can be expressed as

$$P_O = (V_{DS} - V_{DSAT})\, I_D/2$$

where V_{DS}, V_{DSAT}, I_D are the supply voltage, saturation voltage, and current between the drain and source, respectively.

High current is necessary in the low voltage and high power operation, so the total gate width should be increased and V_{DSAT} be minimized as possible as we can. The V_{DSAT} decreases with the decreasing of R_{ON}.

2.2 High Frequency Performance

The high frequency performance can be expressed as

$$G_P = (f_{MAX}/f)^2$$

$$f_{MAX} = f_T/[\,4g_{DS}(R_{CH} + R_S + R_G + \pi f_T L_S) + 4\pi f_T C_{GD}(R_{CH} + R_S + 2R_G + 2\pi f_T L_S)\,]^{1/2}$$

$$f_T = g_m/(2\pi(C_{GS} + C_{GD}))$$

where G_P is the power gain; f_{MAX} is the maximum oscillation frequency; f_T is the cut-off frequency; g_m is the transconductance; g_{DS} is the drain-source conductance; R_{CH} is the channel resistance; R_S is the source resistance; R_G is the gate resistance; L_S is source inductance; C_{GS} is the gate-source capacitance and C_{GD} is the gate-drain capacitance. According to these equations, in order to improve high frequency performance of power VDMOSFET, C_{GS}, C_{GD}, R_{CH}, R_S, R_G should be reduced as possible as we can.

Using the terraced gate structure and Mo gate technology, we can fabricate high performance power VDMOSFETs. The cross section of the high performance VDMOSFET is shown in Fig. 1. The thickness of oxide films under the gate electrode is different as they over the source, channel, and the drain region. A terraced shaped thick oxide layer over the drain region can reduce the gate-drain Miller capacitance C_{GD}. The oxide film over the source region is three times thicker than that over the channel, owing to the enhanced oxidation rate of the heavily doped source region[5]. The increased thickness can also reduce C_{GS} of the device. The Mo gate is employed to reduce the gate resistance. Because the sheet resistance of Mo film is much lower than that of polysilicon, G_P is much improved due to the significant reduction in gate RC time constant and the input power that is dissipated to drive the gate[6,7].

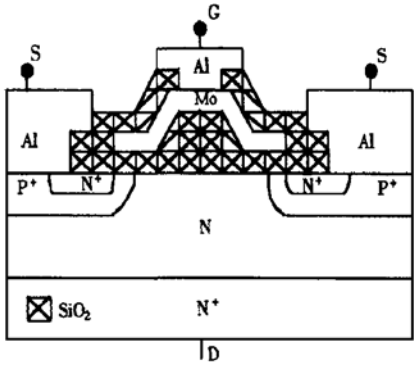

FIG. 1 Cross Section of the VDMOSFET

3 Fabrication and Experimental Results

The high performance power VDMOSFETs studied in this paper were of interdigital cell geometries. N on N^+ substrate epitaxial wafers with (100) crystal orientation were used as starting material. The thickness and resistivity of the epitaxial layer and the lateral dimensions of the cell were optimized to minimize R_{ON} and suit the low voltage application. The gate oxide was thermally grown to be of the thickness of 110nm by using $H_2 + O_2$ oxidation at 970℃. The channel

length of 1.3μm was realized by precise control of the implantation of B^+ and As^+ ions. The terraced shaped thick oxide layer over the drain region was 0.8μm. A SEM photograph of the terraced gate structure is shown in Fig. 2. An interdigital structure was employed with a finger pitch of 20μm. The gate was 6cm in total width, and the chip was 1.83mm × 1.09mm in size. The chip was assembled in a HQ-1 package. The I_D-V_{DS} characteristic of the fabricated VDMOSFET is shown in Fig. 3. It can be seen that the R_{ON} is 0.8Ω when V_{GS} = 10V; the maximum transconductance g_m is 0.7S and the drain current I_D is 1.75A when

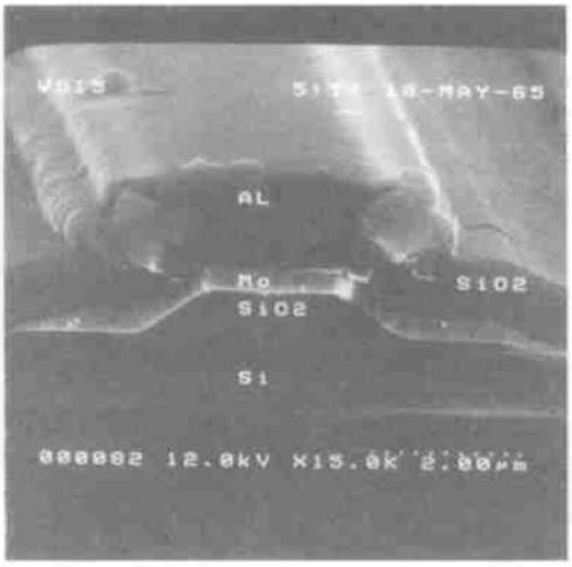

FIG. 2　SEM Photograph of Terraced Gate Structure

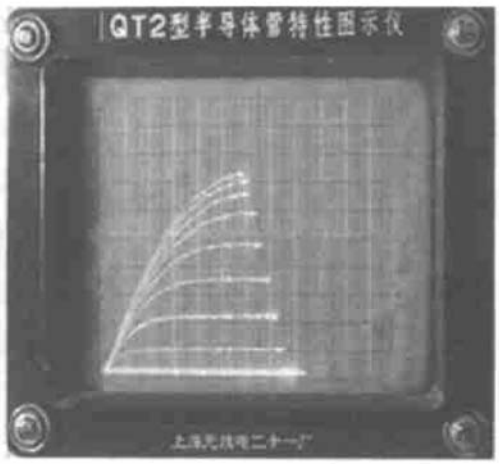

FIG. 3　Typical I_D-V_{DS} Characteristics of Device
I_D: 0.5A/div, V_{DS}: 1V/div, V_{GS} in 1V Step

V_{DS} = 4V while V_{GS} = 5V. The RF performance of the fabricated device is shown in Fig. 4. The output power of 12W with 12dB's gain and 70% drain efficiency have both been obtained.

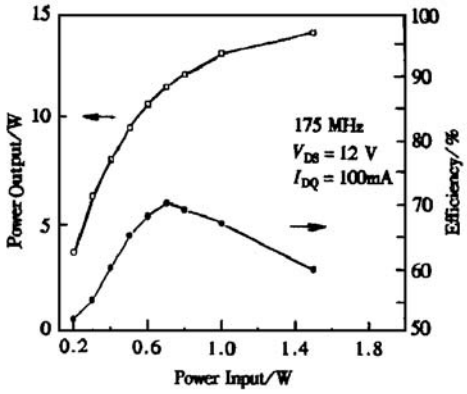

FIG. 4　Power Output and Efficiency vs Power Input

4 Conclusion

A high performance VHF power VDMOSFET suitable for the low voltage operation is fabricated. The terraced gate structure and Mo gate technology is very significant in the reduction in parasitic capacitance and gate series resistance. The device can deliver the output power of 12W with the drain efficiency of 70% and 12dB's gain at 175MHz when V_{DS} = 12V. Devices with excellence performance such as high efficiency and high power gain are possible to be applied widely in VHF band.

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低压应用的高性能甚高频功率 VDMOSFETs

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摘 要: 采用梯形栅结构和难熔金属钼栅工艺, 研制出了高性能, 低电压工作, 适用于移动通信的甚高频功率 VDMOS 场效应晶体管. 该器件在 175MHz、12V 低电压工作条件下, 输出功率为 12W, 漏极效率为 70%, 功率增益为 12dB.

关键词: 低压; 梯形栅结构; 钼栅工艺; 甚高频功率 VDMOSFET
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