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Analytical Model of Surface Field Distribution and Breakdown Voltage for RESURF LDMOS Transistor*

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Abstract: An analytical model of the surface field distribution and breakdown voltage of the reduced surface field lateral double diffusion MOS transistor is proposed. Based on the 2-D Poisson's equation solution, the derived model gives the closed form solutions of the surface potential and electrical field distributions as a function of the structure parameters and drain bias. A criterion for obtaining the optimal trade-off between the breakdown voltage and on-resistance is also presented to serve to quantify the maximum breakdown voltage and optimal relations of all design parameters. Analytical results are shown in good agreement with the numerical analysis obtained by the semiconductor device simulator MEDICI and previous reported experimental data.

Key words: RESURF principle; LDMOS power transistor; breakdown voltage; surface field; on-resistance; optimum design

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1 Introduction

In recent years, Reduced Surface Field (RESURF) technology has been widely used in high-voltage, low on-resistance lateral power devices such as Lateral Double Diffusion Metal-Oxide-Semiconductor transistor (LDMOS), Lateral Insulated Gate Bipolar Transistor (LIGBT), Junction Field Effect Transistor (JFET) and dielectrically isolated devices for implement of the High-Voltage-Integration Circuits (HVIC's) and Smart Power Integration Circuits (SPIC's). Previous many numerical analysis works have fairly well discussed the influence of various parameters on the breakdown voltage and on-resistance, and several models have been proposed for determination of optimal epilayer thickness and doping concentration, drift region length and substrate doping concentrations[1—4].

However, the previous numerical analysis were just completed for some especial structures and all developed analytical models were also based on the approximate 1D Poisson equation solution or some especial assumptions[5—7]. Because of the two-dimensional distribution characteristics of the electrical field in the drift region, any 1D analysis could only figure out an approximate contour of the breakdown characteristics of the RESURF devices. Therefore, the correction and accuracy of those approximations and assumptions need to be further proven for the general case. To our knowledge, there has been no any 2D analytical solution for the

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surface field of RESURF structure LDMOS so far.

This work is to develop a 2D analytical model for calculating the surface field distribution and breakdown voltage of the RESURF LDMOS transistor, based on the Poisson's solution. From this analysis, the surface field and potential distributions have been expressed in terms of the drift region length, epilayer layer doping concentration and thickness and substrate doping concentration. The quantified optimum criterion for the maximum breakdown voltage and lower on-resistance has also been obtained. Analytical results show in good agreement with the numerical analysis and previous reported data.

2 Analytical Model

In present analysis, the simplified investigated structure is shown in Fig. 1. As shown in this figure, the drift region length of the RESURF LDMOS transistor is defined as the n type region length L between the n^+ drain and p^+ well. The epilayer thickness is t_1 with a uniform doping concentration N_d. Assuming the substrate is too thick enough to deplete the substrate charge, the substrate depletion layer thickness is t_2, with doping concentration N_{sub}. t_f is the thickness of the field oxide layer with the dielectric constant of ϵ_{ox}. x and y measure the horizontal and vertical positions relative to silicon surface, respectively. The device is biased in the off-state configuration; substrate, source and gate are grounded while the drain is biased to a positive voltage V_d.

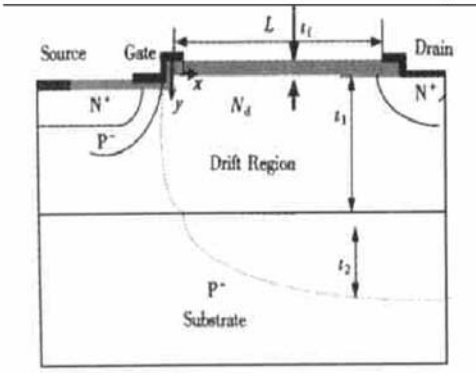

FIG. 1　Cross-Section of RESURF LDMOS Transistor

The potential function $\Phi(x, y)$ in the silicon film must be satisfied by Poisson equation, yielding:

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi(x,y)}{dy^2} = -\frac{qN_d}{\epsilon_{Si}} \tag{1}$$

The region under investigation is the box drift region. It is possible to derive from the 2D Poisson equation a 1D equation describing the surface potential in the lateral coordinate (x). In this work, a more general analysis based on the theory of Reference[8] integrates the Poisson equation over the y-direction in the drift region.

$$\int_0^{t_{Si}} \frac{\partial^2\Phi(x,y)}{\partial x^2}dy + E_y(x,0) - E_y(x,t_1) = -\frac{qN_d}{\epsilon_{Si}}t_1 \tag{2}$$

where for the purpose of analytical investigation, the effect of the junction depth is neglected.

Under the assumption of a 1D electrical field in the SiO_2 material, the continuity of electric flux along the front-Si/SiO_2 interface makes the boundary conditions for (2) satisfy

$$E_y(x,0) = -\frac{\epsilon_{ox}}{\epsilon_{Si}} \times \frac{\Phi(x) - V'_{gs}}{t_f} \tag{3}$$

where $\Phi(x) \equiv \Phi(x, 0)$, is the potential function along the front Si/SiO_2 interface. $V'_{gs} = V_{gs} - V_{FB,f}$, is the effective gate-to-source bias voltage, here $V_{FB,f}$ is the channel flat-band voltage.

Because the gate oxide layer and substrate bias equal zero, neglecting the influence of the work function difference between the metal and semiconductor on the electrical field, the electric field at the Si/SiO_2 interface can be expressed by

$$E_y(x,0) = -\frac{\epsilon_{ox}}{\epsilon_{Si}} \times \frac{\Phi(x)}{t_f} \tag{4}$$

From (2) to (4), one obtains

$$\int_0^{t_{Si}} \frac{\partial^2\Phi(x,y)}{\partial x^2}dy - \frac{\epsilon_{ox}}{\epsilon_{Si}} \times \frac{\Phi(x)}{t_f} - E_y(x,t_1) = -\frac{qN_d}{\epsilon_{Si}}t_1 \tag{5}$$

The relation between $\Phi(x)$ and $\Phi_B(x)$ is derived by solving the continuity equation of the electric flux in the vertical direction

$$\frac{2(\phi_f - \phi_b)}{t_1} = \frac{2\phi_b}{t_2} = E_y(x, t_1) \quad (6)$$

where $\phi_b(x) \equiv \phi(x, t_1)$, is defined as the electrostatic potential at the metallurgical junction of the vertical n^-/p^- junction. From equation (6), we can directly express $E_y(x, t_1)$ as a function of the surface potential and depletion layer thickness.

According to the RESURF principle, the epilayer should be completely depleted and the depletion approximation is suitable for the drift region. At the first-order approximation, we can assume $\frac{\partial^2\phi(x,y)}{\partial x^2} \approx \frac{\partial^2\phi(x)}{\partial x^2}$. Putting everything into (2) and making further mathematics simplification, (2) transforms into the 1D differential equation:

$$\frac{d^2\phi(x)}{dx^2} - \alpha_f\phi(x) = \beta_f \quad (7)$$

with $a_f = \frac{2\epsilon_{ox}}{t_1 t_f \epsilon_{Si}} + \frac{2}{t_1(t_1 + t_2)}$ and $\beta_f = -\frac{qN_d}{\epsilon_{Si}}$.

In order to determine depletion layer thickness in the substrate side, one must solve Poisson equation of the double-sided pn junction along the vertical direction. Due to the little non-uniformity of the substrate depletion thickness along the drift region length direction, we can assume a uniform depletion thickness at first-order approximation. In this case, the depletion thickness within the substrate can be evaluated by using one dimension Poisson equation for the vertical direction drain voltage at the drain region edge. Similar to equation (6), neglecting the influence of the junction depth of the drain region, t_2 can be included in the following form based on the general formulae for the double-sided junction

$$E_{y(x,t_1)_{max}} = \frac{2(V_d - \phi_b)}{t_1} = \frac{qN_{sub}t_2}{\epsilon_{Si}} \quad (8)$$

Based on the basic theory of the pn junction, $\phi_b(x)$ can be simplified expressed into

$$\phi_b(x) = \frac{qN_{sub}}{2\epsilon_{Si}}t_2^2 \quad (9)$$

Combination (8) with (9), a quadric equation gives

$$\frac{t_2}{t_1} = \frac{1}{2}\left(\sqrt{1 + \frac{8\epsilon_{Si}V_d}{qN_{sub}t_1^2}} - 1\right) \quad (10)$$

It is evident that t_2 tends to zero when the substrate doping concentration N_{sub} tends to a very high value such as infinity. The above form is applicable only when the drain voltage makes the depletion width larger than t_1. In general, the high drain voltage at the off state makes the epilayer to be depleted enough. Therefore, the above analysis always exists well.

Solving (7) with boundary conditions $\phi(0) = 0$ and $\phi(L) = V_d$ and defining $\theta_f = -\frac{\beta_f}{\alpha_f}$ and $\tau_f \equiv (1/a_f)^{1/2}$ gives

$$\phi(x) = \theta_f + \frac{(V_d - \theta_f)\sinh\left(\frac{x}{\tau_f}\right) - \theta_f\sinh\left(\frac{L-x}{\tau_f}\right)}{\sinh\left(\frac{L}{\tau_f}\right)} \quad (11)$$

The surface field distribution along the semiconductor surface is obtained by differentiating (11)

$$E(x,0) = -\frac{d\phi}{dx} = -\frac{(V_d - \theta_f)\cosh\left(\frac{x}{\tau_f}\right) + \theta_f\cosh\left(\frac{L-x}{\tau_f}\right)}{\tau_f\sinh\left(\frac{L}{\tau_f}\right)} \quad (12)$$

3 Results and Discussion

Based on the above analysis, the potential and electric field distributions along the semiconductor surface can be readily demonstrated. And the effect of the field oxide layer and silicon film structure on the potential and field can also be analyzed. In order to verify the proposed model, the 2D device simulation is performed using MEDICI for the same structure[9].

Figure 2 shows the analytical results of the surface potential and field distributions obtained from equations (11) and (12) for one RESURF LDMOS transistor together with the simulation results. In the figure, the curves denote the analytical results and the black points represent the numerical results, respectively. A fairly accordance between the analytical and numerical simulation results may be found in general. The discrepancies

between both are due to the penetration of the space charge region into p^+ base region and n^+ drain diffusion region as can be seen from the surface potential and field at $x = 0$ and $x = L$. However, this kind of discrepancies has a little effect on the breakdown voltage analysis.

Curve *a* in Fig. 2 indicates that the potential distribution along the silicon surface is similar to the combination of the $p^+ n^-$ and $n^+ n^-$ abrupt junctions. The total potential drop at the both junctions coincides with the applied voltage.

Curve *b* in Fig. 2 shows the electrical field distribution along silicon film surface. It is evident that there are two edge electric field peaks along the silicon surface, one appears at the $p^+ n^-$ junction interface and the other at the $n^+ n^-$ junction interface. This coincides with the present and previous numerical analysis results[1,2]. Meanwhile, it can be found that the relative magnitude of the two edge peak fields is equal each other. This is because the all structure parameters satisfy the optimal condition, as shown by Colak´ results[3].

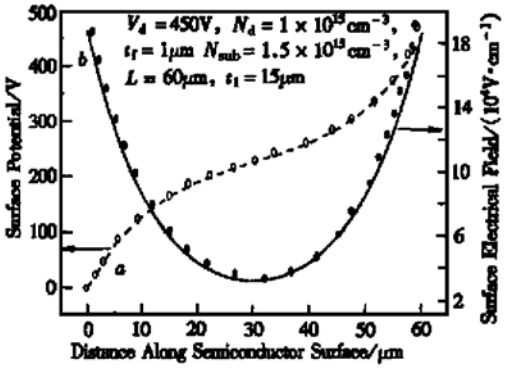

FIG. 2　Surface Potential and Electrical Field Distribution Along Semiconductor Surface

In the design of RESURF LDMOS devices, the epilayer thickness, doping concentration in the drift region, drift region length and field oxide layer thickness are of very importance which determine the off-state breakdown voltage and forward conduction characteristics of the devices. The following discussion will give which optimum relationship.

Based on the expression of the surface electrical field given by (12), utilizing the critical breakdown electrical field concept $E_{max}(x) = E_c = 2 \times 10^5$V/cm can directly evaluate the breakdown voltage for the different drift region doping concentrations. Meanwhile, the drift region on-resistance per-unit width is also evaluated from the expression obtained by Cloak[3,4]. One can observe there exists an optimal epilayer doping concentration at which the maximum breakdown voltage happens and the lower on-resistance is obtained, as shown in Fig. 3. The characteristics of the breakdown voltage versus epi-layer doping concentration curve are similar to the results given by Apples[2]. Moreover, the analytical results show in good agreement with the experimental results obtained by Cloak[3], as shown by the solid point. The quite similar phenomena can also be found for the different epilayer thicknesses, substrate doping concentrations and field oxide layer thicknesses based on our analytical model.

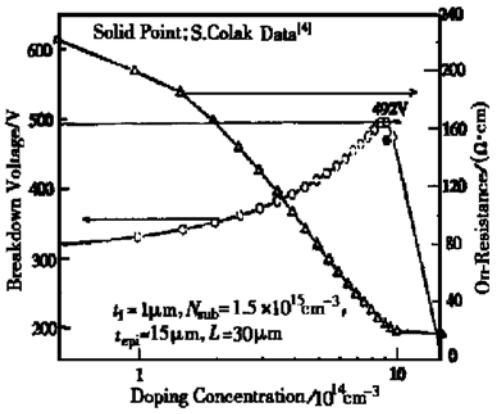

FIG. 3　Trade-off Between Breakdown Voltage and On-Resistance as Function of Drift Region Doping Concentration

The careful examination for the optimal condition of the maximum breakdown voltage and lower on-resistance finds an optimal point where the all parameters make the two surface peak fields equal to each other. Thus, utilizing this analysis, the optimal relationship between the silicon film structure

parameters such as the critical doping concentration and silicon film thickness and the field oxide layer thickness for the optimum design can be obtained and some useful conclusions can be drawn.

4 Conclusion

In this paper, the surface field distribution and breakdown voltage of the RESURF LDMOS devices have been studied analytically. The optimum designed condition, at which the ideal electrical field distribution for the maximum breakdown voltage has also been examined. The analytical calculation results are in good agreement with the numerical simulations and experimental data reported, showing the validity of the analytical expression presented here.

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RESURF LDMOS 功率器件表面场分布和击穿电压的解析模型*

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摘要: 提出了 RESURF LDMOS 功率器件的表面电场分布和击穿电压的解析模型. 根据二维泊松方程的求解, 得到了与器件参数和偏压相关的表面电场和电势分布解析表达式. 在此基础上, 推出了为获得击穿电压和比导通电阻最好折中的优化条件. 该解析结果与半导体器件数值分析工具 MEDICI 得到的数值分析结果和先前的实验数据基本一致, 证明了解析模型的适用性.

关键词: RESURF 原理; LDMOS 功率器件; 表面场分布; 击穿电压; 比导通电阻; 优化设计

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何 进 男, 博士后, 目前研究方向为深亚微米 MOS 器件、功率 MOS 器件、深亚微米 MOS 新结构的设计和表征等.

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