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Characterization of Sub-100nm MOSFETs with High *K* Gate Dielectric*

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Abstract: The short-channel performance of typical 70nm MOSFETs with high *K* gate dielectric is widely studied by using a two dimensional (2-D) device simulator. The short-channel performance is degraded from the fringing field and lower the source/drain junction resistance. The sidewall material is found very useful to eliminate the fringing-induced berrier lowing effect.

Key words: high *K* materials; gate dielectrics; MOSFET
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1 Introduction

With SiO_2 acting as a gate dielectric, the continued scaling down of MOSFETs to sub-100nm is facing a challenge. The thickness of the gate oxide in sub-100nm MOSFETs is designed to be mere 1.5nm; the electrons thus can tunnel the gate oxide easily, as can increase the static power and affect the circuit's operation. An alternative solution is to use high *K* dielectric materials[1], which is of higher dielectric constant, as the much thicker gate dielectric in the same electric field. The studies of the alternative gate oxides began in 1960. Presently, much researches have been carried out with some theoretical and experimental results obtained[2—7].

However, the performance of MOSFET with high *K* dielectric has not been improved; and its characteristics should be further studied in details. Simulations have been done to study the impact of high *K* dielectric materials on the deep sub-100nm MOSFETs[8—10]. The Fringing-Induced Barrier Lowing (FIBL) is used to describe the effect of degradation in device's turn/off on the characteristics of sub-100nm MOSFET with high *K* gate dielectric materials[10]. However, much attention is focused on the study of influence of fringing electric field on the channel instead of on the systematic simulation of the impact of high *K* dielectric on the whole MOSFET. In this work, extensive simulations are carried out to study the impacts of high *K* dielectric on both the channel and the source/drain extension region in a typical 70nm MOSFET. The key factors affecting the device characteristics have been investigated. The different structures of high *K* gate dielectric MOSFETs are

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also simulated.

2 Simulation

The simulations are carried out with a two-dimensional device simulator ISE. The simulated structures are in the typical nMOSFET proposed by NTRS[11], whose gate length and effective gate oxide are 70nm and 1.5nm, respectively. The dielectric constant of the gate dielectric varies from 3.9(SiO_2) to 200 ($BaSrTiO_3$). In order to keep the gate oxide capacitance C_{ox} constant with the dielectric permittivity varying from 3.9 to 200, the thickness of high K gate dielectric is calculated by using $T_K = KT_{SiO_2}/3.9$, where K is the permittivity of high K dielectric and T_{SiO_2} is the equivalent thickness of SiO_2, which keeps 1.5nm during the simulation. The steep retrograde channel profile is used, with a surface doping concentration of $3\times10^{17}cm^{-3}$ and a peak concentration of $5\times10^{18}cm^{-3}$ at the depth of 25nm. The source/drain extension and deep source/drain junction are 25nm and 80nm in depth, respectively. The different structures of sidewall will be described in the next section.

3 Result and Discussion

3.1 Characteristics of MOSFET with High K Gate Dielectric

Figure 1 shows the I-V characteristics of MOSFET with a high K gate dielectric. The insert in Fig. 1 plots the leakage current and saturation current varying with gate dielectric permittivity. From Fig. 1, it can be seen that with K increasing, the leakage current I_{off} becomes larger and the threshold voltage (V_t) becomes lower, while the sub-threshold swing (S) is increased. The source-drain saturation current is also observed to be increased at a higher K. Figure 2 plots the potential distribution along the channel of a 70nm MOSFET with a high K gate dielectric. It reveals that the degradation in the sub-micron MOSFET with a

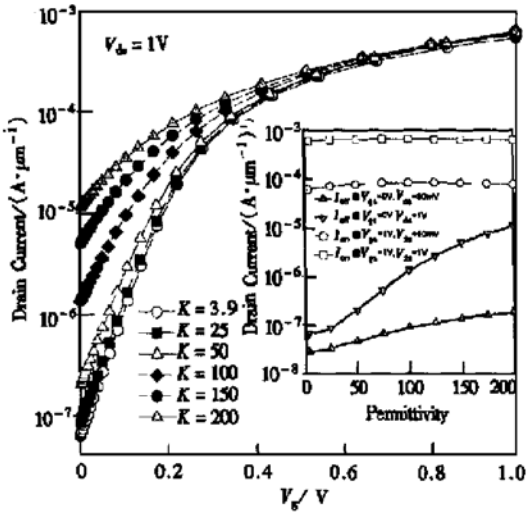

FIG. 1 I-V Characteristics of 70nm MOSFET with High K Gate Dielectric

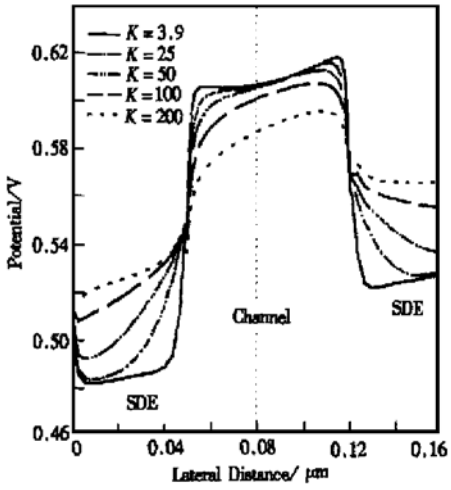

FIG. 2 Potential Distribution Along the Channel of 70nm MOSFET with High K Gate Dielectric

high K gate dielectric can be described as FIBL[8]. It can be seen that with K increasing, the potential difference along the channel decreases, while that in the S/D extension region increases. And the potential barriers of both source and drain junction are lowered. It is because that in order to keeps the gate oxide capacitor C_{ox} constant, the thickness of the gate dielectric T_K has to increase with the K increasing. At a small permittivity, T_K is small compared with the gate length, and the gate oxide ca-

pacitance can be treated as a perfect planar capacitor without any fringing electric field influence. When K increases, T_K becomes larger and is comparable to the gate length, thus the gate oxide capacitance cannot be treated as a perfect planar capacitor any more, and the influence of fringing electric field has to be considered. The fringing electric field can lower the electric field in the channel region but increase that in the source/drain extension region. Consequently, a lower potential barrier of source/drain junction is formed. The higher K corresponds to the thicker T_K, so the impact of fringing electric field becomes more important. Hence, lower potential barrier may decrease the threshold voltage but increase the sub-threshold swing and leakage current. However, the increased electric field in the source/drain region can cause an electron accumulation in these areas, and thus the source/drain junction resistance is reduced. Therefore, the source-drain current becomes larger with a lower source/drain junction resistance.

From the simulation results above, allowing for the influence of fringing electric field, very high K (such as $K = 200$) dielectric is not a suitable candidate to substitute SiO_2 as the gate oxide.

3.2 Characteristics of MOSFET with Different Sidewall Structures

The characteristics of high K gate dielectric MOSFETs with different sidewall structures are simulated by using ISE. In the simulation, the sidewall is made of high K materials. The structure of sidewall with different material is simulated below. Figure 3 shows the I-V characteristics of the MOSFET with an SiO_2 sidewall. In Fig. 3, different sidewall structures are plotted, where structure A is the MOSFETs with a full high K material (the same structure as that simulated in section 3.1); structure B is that with a high K gate dielectric and SiO_2 ($\epsilon = 3.9$) sidewall. It can be seen that when the material of sidewall becomes SiO_2, the fringing electric field effect is decreased accordingly. Figure 4 plots the potential distribution along the channel

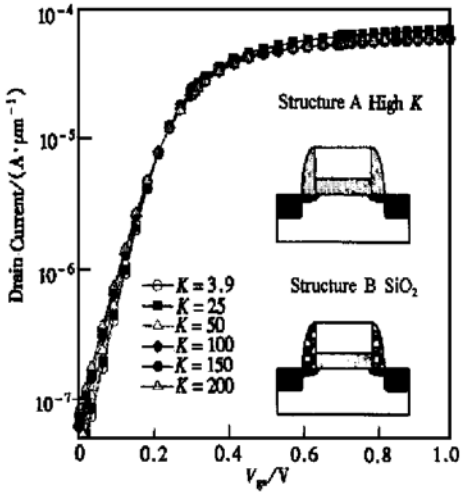

FIG. 3　I-V Characteristics of MOSFET with SiO_2 Sidewall　In the insert, different sidewall structures are plotted.

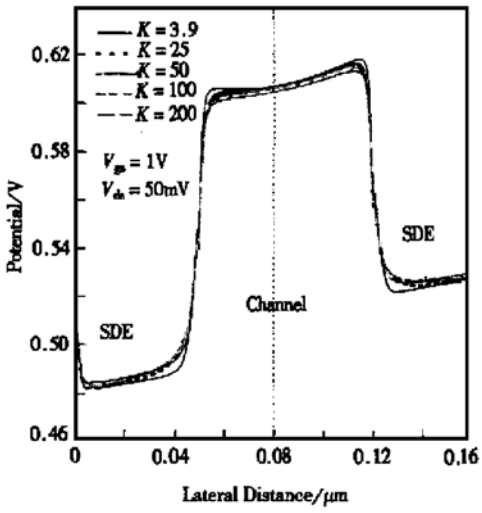

FIG. 4　Potential Distribution Along the Channel of MOSFET with the SiO_2 Sidewall

of MOSFET with the SiO_2 sidewall. Comparing Fig. 2 with Fig. 4, it can be seen that, when the sidewall is changed from a high K material to SiO_2, the potential distribution along the channel will decrease slightly with the increase of K and the potential barriers of source and drain junction be lowered slightly. Thus the FIBL effect can be suppressed by lowering the dielectric permittivity of the material SiO_2. Figures 5 and 6 show the comparison of the characteristics between MOSFET's

with different sidewall materials. Figure 5 shows the impacts of leakage current and saturation current of MOSFET with different sidewall material, while Fig. 6 plots the impact of threshold voltage and subthreshold swing of MOSFETs, where ΔV_{th} is the threshold voltage shift and S is the subthreshold swing. As for structure B, when K increases, no threshold voltage is found to decrease rapidly, while the subthreshold swing and the leakage current are found to increase slightly. Hence, when high K materials are adopted as the gate dielectric, the sidewall materials are very useful to suppress the FIBL effect.

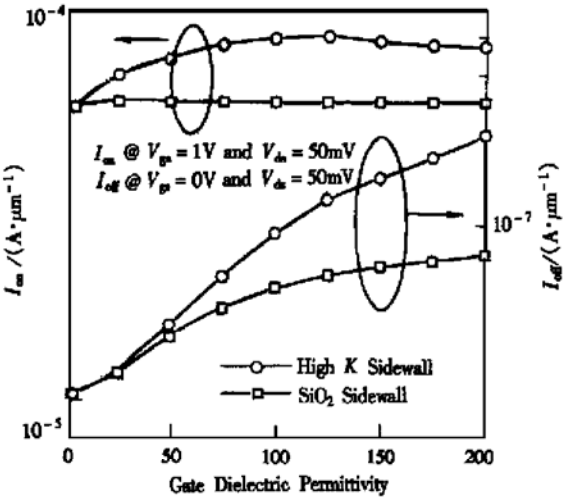

FIG. 5 Impact of Leakage Current and Saturation Current of MOSFET with Different Sidewall Materials

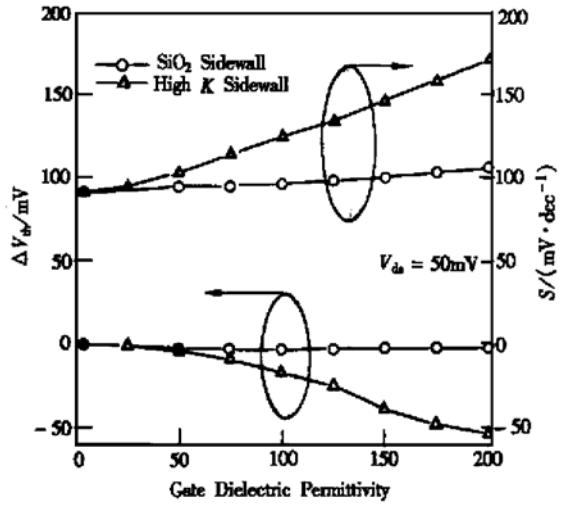

FIG. 6 Impact of Threshold Voltage and Subthreshold Swing of MOSFET with Different Sidewall Materials

4 Conclusion

The MOSFETs with high dielectric permittivity material are simulated by a two-dimensional device simulator. Due to the FIBL effect, when the gate dielectric permittivity increases, the threshold voltage decrease, while the leakage current and the subthreshold swing increase. However, this kind degradation can be suppressed by changing the materials of sidewall.

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亚 0.1 m 高 *K* 栅介质 MOSFETs 的特性

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摘要: 用二维模拟软件 ISE 研究了典型的 70nm 高 *K* 介质 MOSFETs 的短沟性能. 结果表明, 由于 FIBL 效应, 随着栅介质介电常数的增大, 阈值电区减小, 而漏电流和亚阈值摆幅增大, 导致器件短沟性能退化. 这种退化可以通过改变侧墙材料来抑制.

关键词: 高 *K* 材料; 栅介质; 金属-氧化物-半导体场效应晶体管

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