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Substrate Hot Holes Injection Induced Breakdown Characteristics of Thin Gate Oxides*

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Abstract: A substrate hot holes injection method is used to quantitatively examine the roles of electrons and holes separately in thin gate oxides breakdown. The shift of threshold voltage under different stress is discussed. It is indicated that positive charges are trapped in SiO_2 while hot electrons are necessary for SiO_2 breakdown. The anode holes injection model and the electron traps generation model is linked into a consistent model, describing the oxide wearout as an electron-correlated holes trap creation process. The results show that the limiting factor in thin gate oxides breakdown depends on the balance between the amount of injected hot electrons and holes. The gate oxides breakdown is a two-step process. The first step is hot electron's breaking Si—O bonds and producing some dangling bonds to be holes traps. Then the holes are trapped and a conducted path is produced in the oxides. The joint effect of hot electrons and holes makes the thin gate oxides breakdown complete.

Key words: substrate hot holes; thin gate oxides; charge to breakdown; model
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1 Introduction

As gate dielectrics are getting thinner and thinner with the aggressive scaling down of devices geometries, the long-term reliability and integrity of the oxide layers becomes a primary concern[1,2]. In order to meet future needs for dielectric reliability, detailed physical understanding of the dielectric breakdown mechanism is required for ultra-thin oxides. With the failure mechanism and accurate reliability characterization, the MOSFET technology can be optimized and controlled within a safe limit.

Although this topic has been studied extensively in the past, the mechanism of breakdown has not been thoroughly clarified yet[3—7]. In the proposed anode hole injection model[8,9], the injected electrons can generate some holes at the anode to tunnel back into the oxides. Intrinsic breakdown occurs at a critical hole fluence Q_h. However, no satisfactory physical explanation has been given for the link between the breakdown event and this critical hole fluence. Besides the Q_h model, another model has been suggested independently, in which, the critical density of electron traps under the stress is required to trigger the oxide breakdown[10,11].

In this paper, these two models are considered together to describe the oxide wearout via a elec-

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tron-correlated hole trap creation process, ultimately leading to a breakdown event. The roles of hot electrons and holes in the dielectric breakdown of thin gate oxides have been quantitatively investigated by separately controlling the amounts of the injected hot electrons and holes with the Substrate Hot Holes (SHH) injection method. The joint effect of hot electrons and holes is believed essential to the time-dependent dielectric breakdown in thin gate oxides. Finally, a new physical model has been presented, which provide a new angle to understand the nature of dielectric breakdown.

2 Technique and Devices

P-channel MOSFET's were fabricated in n-well regions. The gate width and gate length of the measured devices were 50μm and 5μm, respectively; the gate oxidation was performed at 850℃ for 30min in dry O_2 and then annealed at 900℃ for 20min in N_2. The gate oxide thickness was 10nm, determined by high frequency C-V measurement. The gate material deposited by LPCVD was polycrystalline. The source regions and drain regions were doped by using ion implement technology, with the implement energy and dose being 20keV and $3\times10^{15}/cm^2$, respectively. Phosphorus was diffused into an active area to adjust the threshold voltage.

The ion implementation was divided into two steps. First, the phosphorus was used to prevent the channel from being penetrated, whose energy and dose were respectively 160keV and $6\times10^{11}/cm^2$. Second, the phosphorus was used to adjust the threshold voltage, whose energy and dose were 50keV and $1\times10^{12}/cm^2$, respectively.

An automated test station used for data measurement and collection in these experiments is shown in Fig. 1. Parameters were measured by using an HP4156B high-precision semiconductor parameter analyzer, which was connected to the probe station and composed of four Source Monitor Units (SMU), two Voltage Source Units (VSU), two Voltage Measurement Units (VMU) and one Pulse Generator Units (PGU). This analyzer could control the electric measurement, record the data and perform the statistical analysis. All experiments were conducted via computer to control HP4156B high precision semiconductor parameter analyzer.

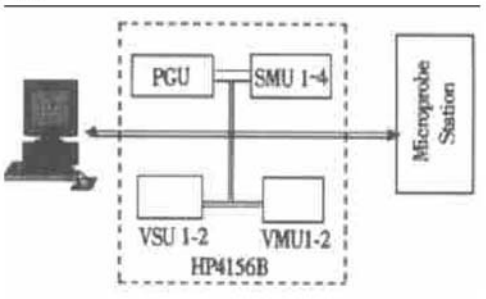

FIG. 1　Block Diagram of Experiment Apparatus

Figure 2 shows the schematic cross section of P-MOSFET used in the SHH injection experiment. Source and drain were grounded in the experiment. The electron current I_e was controlled by the gate voltage, independently of I_e; hole current I_h was controlled by the n-well voltage V_{well} and the p-substrate voltage V_{sub}. The gate current I_g was the sum of I_e and I_h.

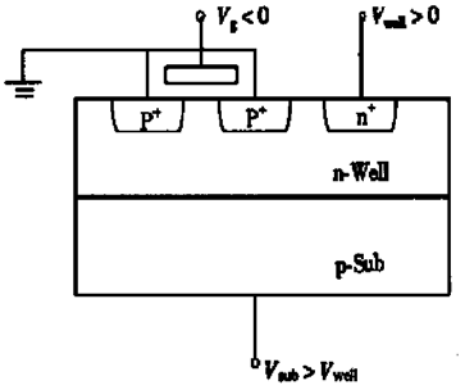

FIG. 2　Schematic Diagram of P-MOSFET

Figure 3 shows the control of V_{bp} to I_g, where the gate current I_g acts as a function of V_{bp} under different gate bias V_g of 10, 10.5 and 11V separately. Here, V_{bp} represents the voltage difference between p-substrate voltage V_{sub} and the n-well voltage V_{well}, i.e. $V_{bp}=V_{sub}-V_{well}$; I_{bp} represents the injection current of pn at the bottom of p-MOS-

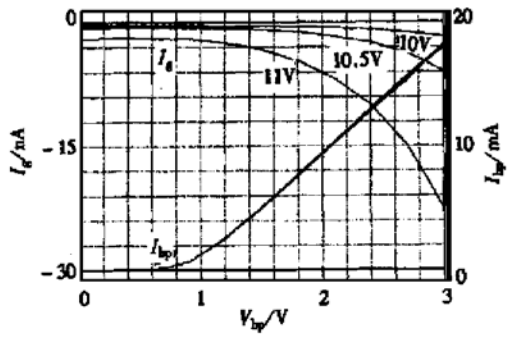

FIG. 3 Gate Current I_g Versus V_{bp} Under Different V_g

FET. If the pn junction is not forward biased, the holes will not be injected into the gate oxide due to the built-in potential between n-well and p-substrate junction. In case I_g is made up of electron current, as long as V_g keeps constant, I_g will keep constant, too, as I_e, which is about - 2nA when the gate oxide voltage V_g= 11V. " - " denotes the current flow out of the device. As the n-well/p-substrate is forward biased (V_{bp} > 0.7V), the holes will be injected from the n-well to gate oxide. The hole current I_h becomes larger with V_{bp} increasing, so does the gate current I_g. The increased component in I_g corresponds with that in hole current I_h. With this technique, we can separately control the amounts of hot electrons and hot holes injected into the gate oxide. Q_e is expressed as below

$$Q_e = J_e \tau_{bd} \quad (1)$$

$$J_e = I_e / S_A \quad (2)$$

where J_e is the injected electron current density; τ_{bd} is the dielectric breakdown time, S_A is the channel area. Similarly, Q_h is expressed as below

$$Q_h = J_h \tau_{bd} \quad (3)$$

$$J_h = I_h / S_A \quad (4)$$

where J_h is the hole current density.

3 Results

We have studied the correlation among Q_h, Q_e and the injected electron current J_e under a constant substrate pn junction voltage V_{bp}, or in other word, in a constant hole current.

Figure 4 shows Q_h and Q_e versus J_e at a constant hole current density of 4×10^{-4} A/cm^2. The electron current J_e varies according to the gate voltage V_g. We can see in Fig. 4 that in a low J_e region, Q_h significantly decreases, so the Q_h model, in which the dielectric breakdown in the gate oxide occurs at a constant hole influence through SiO_2,

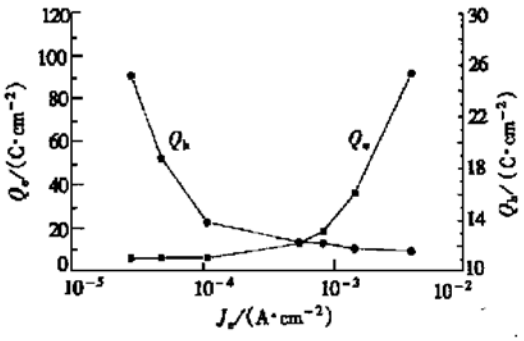

FIG. 4 Q_e and Q_h Versus J_e at Constant J_h

does not hold in the low J_e region; while Q_e keeps almost constant. We can infer from the experimental results that the injected electrons dominate the dielectric breakdown in the gate oxides in the low J_e region. In the high J_e region, Q_h decreases with the increase of J_e and tends to be saturated for the conventional F-N electron tunneling injection. On the other hand, Q_e increases greatly in the F-N tunneling region, though Q_e almost keeps constant in the low J_e region. The experimental results indicate that both injected hot electrons and hot holes are necessary for the dielectric breakdown of gate oxide, either in SHH injection condition or F-N electron injection condition. So, we can assume that hot electrons create hole traps in SiO_2, which lead to the dielectric breakdown after the capture of holes. In the low J_e region, though the amount of injected hot electrons is quite small, they can break Si—O bonds and form some holes traps, so it is the limiting factors for dielectric breakdown in SiO_2. In low J_e region, Q_h is larger than that in high J_e region, due to the lack of injected hot electrons. When the holes traps are sufficiently created by the large amount of injected hot electrons in the high J_e region, especially under F-N electron injection condi-

tions, dielectric breakdown in SiO_2 will be dominated by the total amount of holes injected into the SiO_2, as accords with the Q_h constant region reported by Chen[12].

What's more, we have studied the correlation among Q_h, Q_e and injected electron current J_e in a constant gate oxide field, i. e. a constant hot electron current density. J_h varies with V_{bp}. Figure 5 shows the schematic diagram of Q_e and Q_h as a function of J_h under a constant J_e condition ($J_e = 4 \times 10^{-3} A/cm^2$). We can see that Q_h increases with the hot hole current density J_h increasing in the high J_h region while Q_e maintains constant in this region. It is because there are large amounts of holes passing through the gate oxide without being trapped. In this case, Q_e is constant, because the dielectric breakdown in SiO_2 occurs immediately after the injected hot electrons create the critical amount of hole traps for the SiO_2 dielectric breakdown. On the contrary, it is found that in the low J_h region, Q_e decreases with the increase of J_h, while Q_h is constant. In this case, the amount of injected holes is a limiting factor for the dielectric breakdown. From the experimental research described above, it is deduced that the cooperation of hot electrons and hot holes is necessary for the dielectric breakdown in SiO_2.

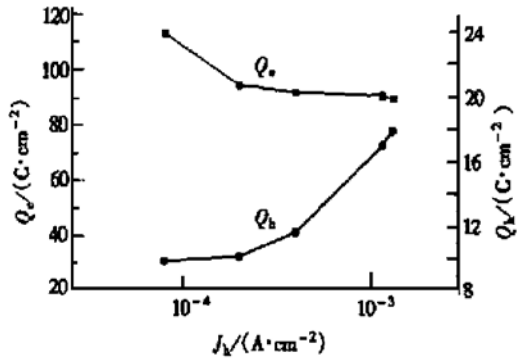

FIG. 5　Q_e and Q_h Versus J_h at Constant J_e

4　New Model for Dielectric Breakdown

The time-dependent dielectric breakdown mechanism of the gate oxide is still under dispute. All kinds of models have been presented to describe the TDDB breakdown, among which, the most important two are the impact ionization model and the electron traps model. Those who support the impact ionization model think that the hole flow is generated because of the impact ionization; when the hole flow reaches some value Q_h, the gate oxide will breakdown. This model is based on the impact ionization, but the gate oxide will also breakdown under a lower voltage if its thickness is less than 10nm. In this case, no impact ionization will happen, as can not be explained by this model. We have made many experiments on PMOSFET's, with the results indicating that Q_h is not a constant but connected with the stress condition. Therefore, to characterize the time dependent dielectric breakdown by using a constant Q_h is just approximate to some extend. The electron traps breakdown mode indicates that the electron traps existing in the gate oxide can capture the electrons and make the electric field increase. When the electric field arrive at a critical value, the breakdown of the gate dielectric will happen. This model can explain many experimental results very well except for the positive charge captured in the oxide.

In order to investigate the roles of electrons and holes in the gate oxide breakdown, we exert different bias on the PMOSFET, with the results shown in Fig. 6. It is found that the increase in the threshold voltage is negative under any bias, so the charge captured in the gate oxide must be positive. The shift of threshold voltage becomes more negative with the stress time increasing, which indicates that more and more positive charges are trapped in the gate oxide with time increasing. From this figure, we can also find that the shift of threshold voltage increases with the increase of stress intensity. Increasing stress intensity makes more hot electrons and traps generated, as leads to the shift of threshold voltage increasing. Much attention should be paid to the curve of biasing voltage when $V_g = 3V$, $V_{bp} = 1.2V$. In this case, the shifts of

threshold voltage are almost zero. This phenomenon shows that not all hot electrons are generated under a low bias. There still exist some holes, which do not be captured because no hot electrons are injected into the gate oxide or no traps are formed. So we conclude that hot electrons are essential conditions of SiO_2 breakdown. The positive drift of threshold proves that the positive charges are trapped in SiO_2. It is considered that there is certain connection between the holes trapped model and the electrons trapped model. Under the condition that the hot electrons are injected into the weak bonds, such as the gate oxide strain Si—O, etc., to produce some silicon dangling bonds acting as hole traps, once the holes are captured by the traps, the trivalent silicon will be generated. When the locally collapsed trivalent silicon structure forms a conductive path in SiO_2, the dielectric breakdown will happen.

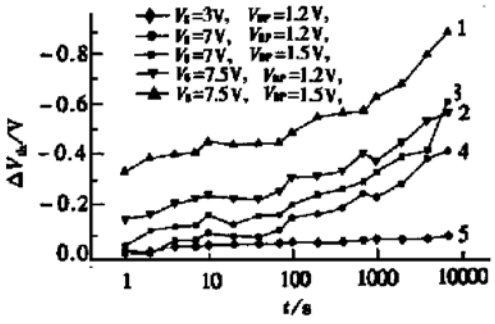

FIG. 6 Shift of Threshold Voltage vs Time

It is well known that Si—O, Si—H and Si—Si weak bonds exist on the interface between gate oxide and Si-SiO_2. In addition, there exist transition regions on the Si-SiO_2 interface. The combination of every two bonds is very weak, which can be separated with little energy. In a high electric field, the weak bonds in the gate oxide, interface and transition region will break to form some traps.

Base on above experiment, a new model for dielectric breakdown in SiO_2 is presented to describe the ultra-thin gate oxide breakdown, which characterize the ultra-thin gate oxide breakdown in two steps. The first step is connected with hot electrons. Hot electrons gain energy from high electric field and are injected into the gate oxide by F-N tunneling. High energy hot electron can break weak bonds, such as Si—O, etc., to form the trap center. The second step is the holes being captured by these traps.

5 Conclusion

The roles of hot electron and holes in dielectric breakdown of the thin gate oxides have been quantitatively investigated in this paper by separately controlling the amounts of injected hot electrons and holes with substrate hot holes injection method. When J_h keeps constant, it can be seen that Q_h decreases with J_e increasing; while Q_e is constant in a low J_e region. When J_e is high, Q_e will increase with J_e increasing and Q_h tends to saturate and keeps constant. This means the dielectric breakdown at Q_h, which acts as a criterion, does not apply to the whole stress process. When J_e keeps constant, similar situation occurs. Moreover, the shift of threshold voltage has been measured. The negative shift value under different stress conditions indicates that the positive value trapped in SiO_2 dielectric and hot electron is necessary for the dielectric breakdown. From the experimental results, a new model for ultra-thin gate oxides breakdown is presented. We presume that the gate oxide breakdown is divided into two steps. One is hot electrons breaking Si—O bonds and producing some dangling binds as holes traps. The other is holes being trapped and a conducted path being produced. In conclusion, the joint effect of electrons and holes makes the ultra-thin gate oxides breakdown complete.

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衬底热空穴注入下的薄栅氧化层击穿特性*

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摘要: 利用衬底热空穴(SHH)注入技术, 分别定量研究了热电子和空穴注入对薄栅氧化层击穿的影响, 讨论了不同应力条件下的阈值电压变化. 阈值电压的漂移表明是正电荷陷入氧化层中, 而热电子的存在是氧化层击穿的必要条件. 把阳极空穴注入模型和电子陷阱产生模型统一起来, 提出了薄栅氧化层的击穿是与电子导致的空穴陷阱相关的. 研究结果表明薄栅氧化层击穿的限制因素依赖于注入热电子量和空穴量的平衡. 认为栅氧化层的击穿是一个两步过程. 第一步是注入的热电子打断 Si—O 键, 产生悬挂键充当空穴陷阱中心, 第二步是空穴被陷阱俘获, 在氧化层中产生导电通路, 薄栅氧化层的击穿是在注入的热电子和空穴的共同作用下发生的.

关键词: 衬底热空穴(SHH); 薄栅氧化层; 击穿电荷; 模型

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