

## Sensitivity Analysis of the Back Interface Trap-Induced R-G Current Obtained by a Lateral SOI Forward Gated-Diode\*

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**Abstract:** The sensitivity analysis of the back interface trap-induced Recombination-Generation (R-G) current of the lateral SOI forward gated-diode is discussed. The dependence of the R-G current sensitivity on the back interface traps is examined in the normalized form and the effects of some key factors such as the silicon film thickness and channel doping concentration are demonstrated. The results show the R-G current is heavily dependent on the interface trap density. The effects on the R-G current magnitude of the channel doping concentration and the silicon film thickness of the SOI devices must also be considered in order to accurately model the interface traps via the R-G current peak.

**Key words:** R-G current; gated-diode; interface traps; SOI-MOSFET; sensitivity

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### 1 Introduction

It is well known that SOI technology is becoming one of the mainstreams in sub-micron and deep sub-micron devices used in high density and low power applications. A key to improve the performance of SOI-based devices and circuits is to reduce the density of electron-hole recombination and the trapping centers at the SiO<sub>2</sub>-Si interface for suppressing leakage current and improving hot carrier reliability and radiation hardness.

However, SOI technology is based on the complicated ultra-thin silicon film on SiO<sub>2</sub> insulation layer fabrication process. Due to the very large buried oxide layer thickness and the multi-layer

isolation, it is very difficult for one to control and measure the buried oxide interface trap properly. Recently, there has been increased interest in the old gated-diode technique, new modifications of which are used to study current bulk CMOS and SOI devices. It has been reported that the R-G current is an effective monitor for characterizing the interface traps and bulk carrier lifetime with the advantages of high sensitivity and fast evaluation<sup>[1-4]</sup>.

In comparison with conventional R-G current measurements of MOSFET and MOSFET/SOI devices, only a few studies have investigated the sensitivity of the R-G current of the gated-diode to the interface trap conditions and the structure parameters. In fact, it is very important for the gated-diode

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measurement to obtain high R-G current sensitivity to the interface traps when characterizing of SOI devices. Our simulations have shown that many factors play important roles in determining the magnitude of R-G current<sup>[5,6]</sup>, which also affect the accuracy of the R-G current method as a monitor technique to characterize the interface traps.

In order to elucidate the above issues and make the gated-diode method better suited for interface trap characterization of the SOI devices, this work performs a comprehensive sensitivity analysis of the gated-diode R-G current to the interface trap conditions and structure parameters through the numerical simulation. Using an SOI lateral gated-diode configuration with a slightly forward bias, the R-G current of the back interface traps has been simulated. The effects of the interface trap density, surface recombination velocity and structure parameters on the R-G current have been examined in a normalized form, and the quantitative sensitivity data are presented in detail.

## 2 Structure and Simulation

The device used in this study is a common SOI lateral gated-diode structure, as shown in Fig. 1. The channel length is chosen as  $10\mu\text{m}$  in order to enlarge the effect of the interface traps.

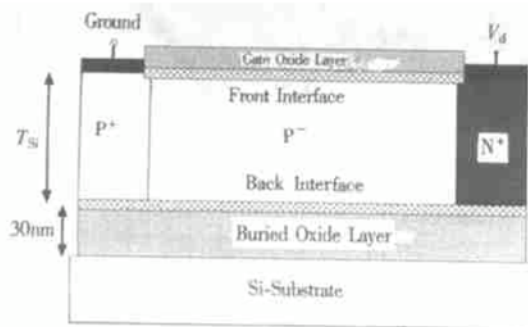


FIG. 1 Cross-Section of SOI Lateral Gated-Diode

The first step is to determine the representative characteristics of the typical process variation. Exact information on manufacturing variations of a device is proprietary. However, most semiconductor manufacturers strive to make all unit process varia-

tions conform to at least  $3\sigma$  value of no more than 5% compared to the standard process module.

Based on this, it is very easy to get reasonable estimates for unit step variations. The interface traps and structure parameters can be chosen in the following manner: center values of the variables adapt the typical device and the variation is within  $\pm 15\%$ . Structure parameters and interface trap variations are given in Table 1. Default parameters used in the simulation are the entry in the center value column unless otherwise noted.

Table 1 Simulation Parameters

Parameters	Center Values	Variations	Units
Channel Doping Concentration $N_{ch}$	$10^{16}, 5 \times 10^{16}, 10^{17}$	- 15% to + 15%	$\text{cm}^{-3}$
$T_{Si}$ Fully-Depleted	60, 80, 120,	- 15% to + 15%	nm
Partially-Depleted	140, 160, 180, 200	- 15% to + 15%	nm
Gate Oxide Thickness	10	0	nm
Buried Oxide Thickness	200	- 15% to + 15%	nm
Back Interface Trap Density	$10^{10}, 5 \times 10^{10}, 10^{11}$	- 15% to + 15%	$\text{cm}^{-2}$
Surface Recombination Velocity ( $s_n$ )	10, 20, 30, 40, 50	- 15% to + 15%	cm/s
Diode Bias Voltage	- 0.4	0	$V_d$

For the sake of simulation, we choose the back interface trap density,  $s_n$ , silicon film thickness, buried oxide thickness and channel doping *et al.*, as the variables, respectively. By using 2-D numerical simulation tool, DESSIS-ISE<sup>[7]</sup>, SOI device behavior can be thoroughly understood.

## 3 Results and Discussion

The sensitivity analysis can be performed with the method chosen based on the above parameter settings. Figure 2 illustrates the sensitivity of the relative R-G current peak on the interface trap density in the normalized form for the fully and partially depleted SOI gated-diode cases.

At first, as shown in this figure, the relative change of the R-G current shows a linear relationship on the interface trap density for the different center values of the interface trap density, which is

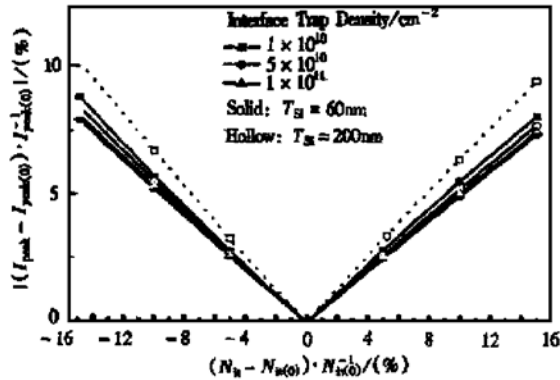


FIG. 2 R-G Current Sensitivity vs Interface Trap Density Variation

in accordance with SRH theory estimation. From here, one can deduce that the R-G current shows high sensitivity to the change of the interface trap density. Secondly, the symmetrical characteristics of the change of the R-G current keep well for either increase or decrease of the interface traps density, which is the nature extension of the linear dependence. Thirdly, in FD and PD cases, for the different center value of the interface traps density, all curves nearly overlap together indicates that the slope of the R-G current almost keep constant except one case of  $1 \times 10^{10} \text{ cm}^{-2}$ . This important result indicates that the varied slope of the R-G current with the interface traps density should obey the quite same linear law either for the FD or PD SOI devices. Finally, one significant feature is that the slope of the R-G change is smaller than one, not expected one. For this phenomenon, it may be contributed to local bulk effect of the interface traps. From the slight scattering of the R-G current for the different interface trap density one can observe a very important fact: the lower the interface trap density, the higher the sensitivity of the R-G current. This phenomenon may be the non-linear dependence of the R-G current on the interface traps, which will be further studied in our next work.

Figure 3 shows the R-G current sensitivity on the variation of the surface recombination velocity for the fully or partially depleted devices. From this

figure, one can find that for either FD or PD SOI device, the sensitivity curves of the R-G current versus  $s_n$  nearly overlap one curve for the different surface recombination velocity. The slope of the R-G current almost keeps one for all cases, showing high sensitivity of the R-G current to the surface recombination velocity. Although the different silicon film thickness makes the magnitude of the R-G current peak adapt different values, the normalized method makes the inherent change law of the R-G current versus  $s_n$  give prominence to one.

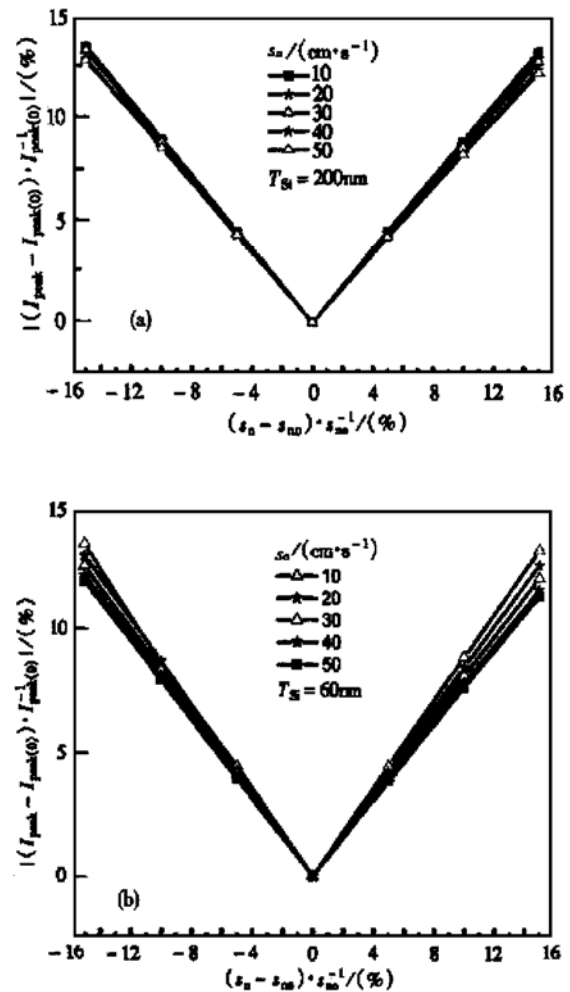


FIG. 3 (a) R-G Current Sensitivity on Variation of Surface Recombination Velocity for Partially Depleted Device; (b) R-G Current Sensitivity on Variation of Surface Recombination Velocity for Fully Depleted Device

Figure 4 shows the sensitivity of the R-G current to the change of the channel doping concentra-

tion. At first, as seen in this figure, the relative change of the R-G current shows a weaker dependent relationship for the different center values of

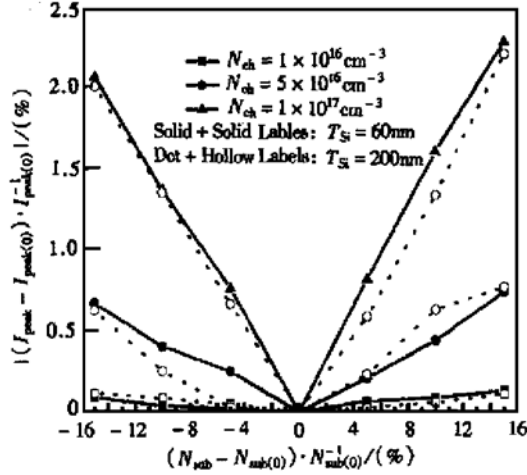


FIG. 4 R-G Current Sensitivity on Variation of Channel Doping Concentration for FD and PD Devices

the channel doping concentration. One can see that the lower the channel doping concentration, the weaker the sensitivity. For example, there is no relation between R-G current of gated-diode and channel doping concentration if the concentration is smaller than  $1 \times 10^{16} \text{ cm}^{-3}$ . Thus, it is very suitable to use the R-G current method of the gated-diode for the low channel doping concentration device characterization, such as the light detectors, to directly extract the interface trap density based on the normal SRH theory. However, for the high channel doping concentration, R-G current is partially dependent on the channel doping concentration, which will result in a significant error in characterizing interface trap density. This phenomenon is due to the Bandgap Narrow Effect (BGN) with the doping simulated by our last paper<sup>[5]</sup>, the magnitude of R-G current including BGN effect is 1.5 factor larger than that without BGN. In this case, BGN effect on extraction of the interface trap density from the measured R-G current must be taken into consideration. For the sub-micron and deep sub-micron devices, the channel doping concentration is increasing up to  $10^{18} \text{ cm}^{-3}$ , this effect

will become more evident.

Moreover, one can observe that above variation is not a linear function with the change of the channel doping concentration. This relation indicates the function between R-G current peak and channel doping concentration is very complex and usually result in converge problem in the simulation. However, this variation amplitude is always within the range of 2% for the 15% variation of the channel doping. It indicates that the change of the R-G current peak due to the channel doping concentration may be neglected in a first order approximation. This will greatly simplify the R-G current modeling and the extraction process.

Figure 5 shows the sensitivity of the R-G current peak on the silicon film thickness. Similar to the channel doping concentration, the sensitivity of the R-G current peak is strongly dependent on SOI device characteristics, such as FD or PD model. With the transformation from the PD to the FD, the sensitivity of R-G current to the silicon film thickness increases. For the ultra-thin SOI devices such as 40nm SOI gated-diode, the sensitivity of R-G current to the silicon film thickness surpass over that of the interface trap density and  $s_n$ . However, this is very rare for the practical SOI technology.

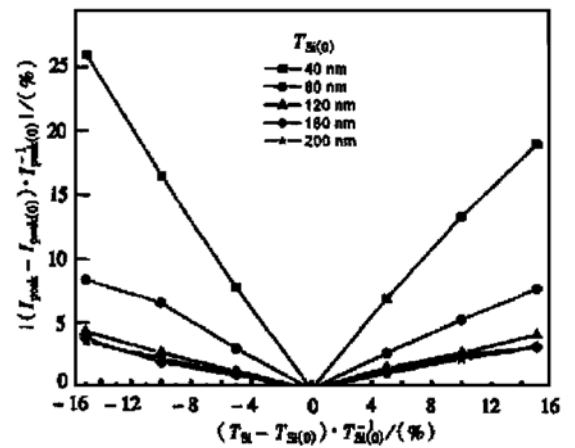


FIG. 5 R-G Current Sensitivity on Variation of Silicon Film Thickness for Fully-Depleted and Partially-Depleted Devices

Moreover, for the PD devices, the sensitivity of the R-G current to the silicon film thickness is

within 5% for the 15% variation of the silicon film thickness. Therefore, this effect is smaller than that of the interface trap density and  $s_n$ , which helps to improve the accuracy of modeling the interface trap effect on the R-G current peak.

Figure 6 illustrates the comparison of the sensitivity of the R-G current peak to the different structure parameters and interface trap density. It is very evident in almost all cases the interface trap

density is the first significant factor for the effect of the R-G current peak sensitivity, the silicon film thickness is the second factor and the channel doping is the smallest one. It should be noted that on the sensitivity of the R-G current peak of the interface trap, the silicon film thickness of FD devices plays a much more important role than that of PD devices.

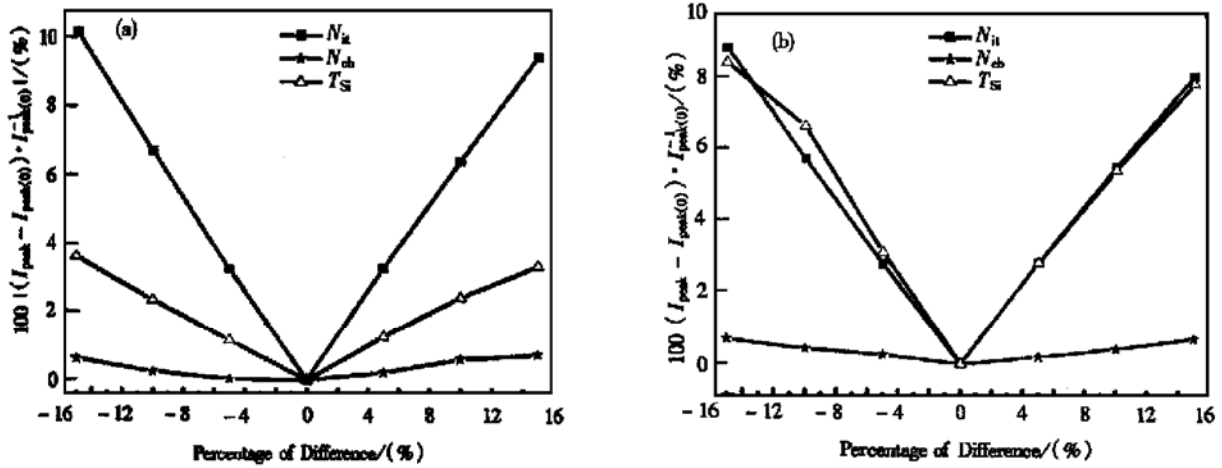


FIG. 6 (a) Comparisons of Sensitivity of R-G Current Between Interface Traps, Silicon Film Thickness and Channel Doping Concentration for Center Values of  $T_{Si} = 200\text{nm}$ , Interface Trap Density  $N_{it} = 10^{10}\text{cm}^{-2}$ ,  $N_{ch} = 5 \times 10^{16}\text{cm}^{-3}$ ; (b) Comparison of Sensitivity of R-G Current Peak to Interface Traps, Silicon Film Thickness and Channel Doping Concentration for Center Values of  $T_{Si} = 60\text{nm}$ , Interface Trap Density  $N_{it} = 10^{10}\text{cm}^{-2}$ ,  $N_{ch} = 5 \times 10^{16}\text{cm}^{-3}$

## 4 Conclusion

In this paper, the sensitivity of the R-G current peak to the structure parameters and back interface trap conditions was analyzed numerically in details. The effects of the different influenced factors on the sensitivity of the R-G current peak were compared. It was shown that the back interface trap density is the most significant factor and the silicon film thickness is the second one in all cases. However, there is difference between FD and PD devices for the sensitivity of R-G current to the silicon film thickness, which should be treated differently in modeling and extracting the interface trap parameters.

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## 栅控二极管 R-G 电流法表征 SOI-MOS 器件埋氧层界面陷阱的敏感性分析\*

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**摘要:** 通过数值模拟手段, 用归一化的方法研究了界面陷阱、硅膜厚度和沟道掺杂浓度对 R-G 电流大小的影响规律. 结果表明: 无论在 FD 还是在 PD SOI MOS 器件中, 界面陷阱密度是决定 R-G 电流峰值的主要因素, 硅膜厚度和沟道掺杂浓度的影响却因器件的类型而异. 为了精确地用 R-G 电流峰值确定界面陷阱的大小, 器件参数的影响也必须包括在模型之中.

**关键词:** R-G 电流; 栅控二极管; 界面陷阱; SOI MOSFET 器件; 敏感性

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