

Current Mismatches in Charge Pumps of DLL-Based RF CMOS Oscillators

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Abstract: A research on the spurious tones due to the current mismatch in charge pumps of DLL (Delay Locked Loop)-based RF CMOS oscillators is performed. An equation for strength evaluation of the spurious tones is derived. Two tables are provided to make it obvious to understand for the characteristics of spurious tones changing with related parameters. Some suggestions are given for the design of a DLL-based RF CMOS oscillators.

Key words: spurious tone; Phase Locked Loop (PLL); DLL; RF CMOS transceiver; Local Oscillator (LO)

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1 Introduction

To implement all the RF functions on a single chip is one approach to dramatically increase integration levels in RF CMOS transceivers^[1]. Local Oscillators (LOs) in transceivers are key building blocks used to shift down a received carrier signal spectrum to a lower frequency, or shift up a signal spectrum to a higher frequency band. To integrate a LO with high quality of phase noise performance in CMOS processes is a severe problem in the RF CMOS transceiver design.

A charge-pump DLL (Delay Locked Loop)-based RF CMOS oscillator, which produces a low-phase-noise RF signal by taking advantage of the inherently low jitter of a low-frequency crystal oscillator reference, is a good choice to implement the integrated LO. In Reference[2], a 900MHz LO using DLL-based frequency multiplier is described. The multiplying is accomplished by taking each relatively jitter-free edge of the crystal oscillator

output and generating a burst of well-controlled evenly-spaced edges which span one period of the crystal oscillator. These evenly-spaced edges form a pattern of higher-frequency transitions and eventually realize the desired RF signal.

Fabricated in a CMOS process, a charge-pump suffers from a problem of "dead zone" due to the failing to turn on the current sources fully when the switches are connected only in a little time interval. To cancel the "dead zone", both the charging current and the discharging current should be high simultaneously for a sufficient amount of time to completely switch on the currents. During this time, the charge on the capacitor will not be changed if the currents are the same in value, namely, the voltage on the capacitor is constant when the loop is locked. However, there is always a few percent of mismatch between the currents when fabricated in CMOS processes. Reasons for such mismatches are process variances, disagreements between simulations and tests, some other power and temperature related issues.

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Current mismatches in charge pumps produce spurious tones around the center output carrier of a DLL-based RF CMOS oscillator. This paper presents a detailed analysis of the current mismatch effect on the DLL-based oscillators.

2 Spurious Tone Analysis

Assuming that the input ports “up” and “down” of a charge pump as illustrated in Fig. 1 are identical and Δt is the time necessary to completely switch on the currents to avoid “dead zone”, during Δt , the charge deposited on the capacitor C_p is

$$Q_c = (I_1 - I_2) \Delta t \quad (1)$$

If $I_1 \neq I_2$, $Q_c \neq 0$. This notes that the V_{con} varies as the changing of the charge deposited on the capacitor in the charge pump. An inversely controlling makes the Q_c towards 0 on account of the loop's negative feedback character. In the end, a phase error $\Delta t'$ between the input ports of the charge pump is produced to compensate Q_c .

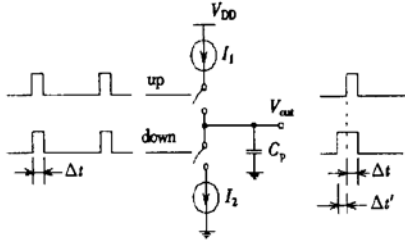


FIG. 1 Charge Pump

$$\Delta t' = \left(\frac{I_1}{I_2} - 1 \right) \Delta t \quad (2)$$

When the charge pump is working in a PLL (Phase Locked Loop), since only one phase error will be added to the output carrier, there will be no spurious tone generated and a phase error is not a drawback to an oscillator if the charge-sharing problem is ignored and the bandwidth of the low pass filter in the DLL is much less than the frequency of the input reference.

In Fig. 2, the output of a DLL-based RF CMOS oscillator is illustrated with $I_1 = I_2$ and $I_1 \neq I_2$, respectively. The multiplier factor is presumed to be N , the period of the input reference is T_{ref} . In

one period of the input reference, the output is defined as $f_0(t)$, illustrated in Fig. 3.

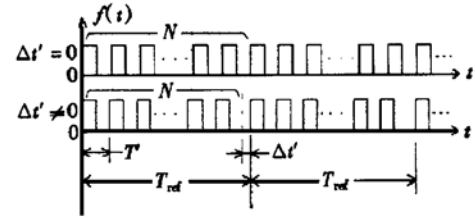


FIG. 2 Output of DLL-Based RF Oscillator

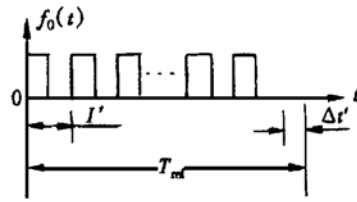


FIG. 3 One Period of Output

$$f_0(t) = \sum_{m=1}^N \{ u[t - mT'] - u[t - (m + 0.5)T'] \} \quad (3)$$

where $T' = \frac{1}{N}(T_{ref} - \Delta t')$, $u(t)$ is step function, then yielding

$$\frac{df_0(t)}{dt} = \sum_{m=1}^N \{ \delta[t - mT'] - \delta[t - (m + 0.5)T'] \} \quad (4)$$

where the $\delta(t)$ is impulse function. The Fourier transform of $\frac{df_0(t)}{dt}$ is $j\omega F_0(\omega)$ ^[3]. So

$$j\omega F_0(\omega) = \sum_{m=1}^N [e^{-j\omega T'm} (1 - e^{-j\frac{1}{2}\omega T'})] = (1 - e^{-j\frac{1}{2}\omega T'}) \sum_{m=1}^N [e^{-j\omega T'm}] \quad (5)$$

$$F_0(\omega) = \frac{(1 - e^{-j\frac{1}{2}\omega T'})}{j\omega} \sum_{m=1}^N [e^{-j\omega T'm}] = \frac{e^{-j\omega T'}(1 - e^{-j\omega N T'})}{j\omega(1 + e^{-j\frac{\omega T'}{2}})} \quad (6)$$

When the $f_0(t)$ is periodically extended, $f(t)$ is gotten as illustrated in Fig. 2. By referring [3], $F(\omega)$, the Fourier transform of $f(t)$ is

$$F(\omega) = 2\pi \sum_{n=-\infty}^{\infty} F_n \delta(\omega - n\omega_{ref}) \quad (7)$$

where $F_n = \frac{1}{T_{ref}} F_0(\omega) \Big|_{\omega=n\omega_{ref}}$, $\omega_{ref} = \frac{2\pi}{T_{ref}}$, F_n is the vector of harmonics of the reference.

$$F_n = \frac{1}{T_{\text{ref}}} F_0(\omega) \Big|_{\omega = n\omega_{\text{ref}}} = \frac{1}{T_{\text{ref}}} \times \frac{e^{-j\omega T'}(1 - e^{-j\omega N T'})}{j\omega(1 + e^{-j\omega T'/2})} \Big|_{\omega = n\omega_{\text{ref}}} = \frac{e^{-j\frac{2\pi P}{N}n}(1 - e^{-j2\pi P n})}{j2n\pi(1 + e^{-j\frac{2\pi P}{N}n})} \quad (8)$$

where $P = \frac{T_{\text{ref}} - \Delta t'}{T_{\text{ref}}} = 1 - \frac{\Delta t'}{T_{\text{ref}}}$, implies the ratio of the delay time of the delay line to the T_{ref} .

When $\Delta t' = 0$, which means $I_1 = I_2$, $P = 1$. One obtains

$$|F_n| = \begin{cases} \frac{1}{2} & n = 0 \\ \frac{1}{\pi(2m+1)} & n = (2m+1)N \\ 0 & \text{others} \end{cases} \quad (9)$$

$$|F_n| = \frac{1}{T_{\text{ref}}} \times \frac{|e^{-j\frac{2\pi P}{N}n}|}{2\pi|jn|} \times \frac{|1 - e^{-j2\pi P n}|}{|1 + e^{-j\frac{2\pi P}{N}n}|} = \frac{1}{T_{\text{ref}}} \times \frac{1}{2\pi} \times \frac{1}{|n|} \times \left[\frac{(1 - \cos 2\pi P)^2 + \sin^2(2\pi P)}{(1 + \cos \pi \frac{n}{N} P)^2 + \sin^2(\pi \frac{n}{N} P)} \right]^{\frac{1}{2}} \quad (10)$$

Let $K_n = 20 \lg \left| \frac{F_n}{F_N} \right|$ (dB) (11)

here K_n , the function of n , N and P , represents the strength ratio of the spurious tones to the fundamental tone, the F_N . Because $N\omega_{\text{ref}}$ is the output frequency of the DLL-Based RF CMOS oscillator, from Eq. (7), F_N is the effect tone we are producing (Fig. 4). Tables 1 and 2 are the calculated results of K_n by computer.

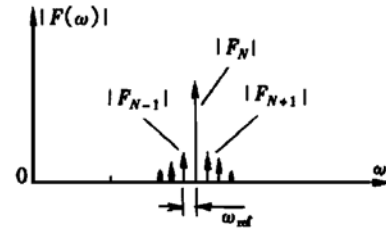


FIG. 4 Output Spectrum

Table 1 K_n (dB) with $N = 40$ and P from $1 - 10^{-4}$ to $1 - 10^{-10}$ Step 10^{-1}

P	$1 - 10^{-4}$	$1 - 10^{-5}$	$1 - 10^{-6}$	$1 - 10^{-7}$	$1 - 10^{-8}$	$1 - 10^{-9}$	$1 - 10^{-10}$
$n - N$							
± 1	- 47.92	- 67.95	- 87.95	- 107.9	- 127.9	- 147.7	- 165.7
± 2	- 53.95	- 73.96	- 93.97	- 113.9	- 133.9	- 153.7	- 171.7
± 3	- 57.46	- 77.47	- 97.48	- 117.4	- 137.4	- 157.2	- 175.2
± 4	- 59.95	- 79.96	- 99.96	- 119.9	- 139.9	- 159.7	- 177.7
± 5	- 61.87	- 81.88	- 101.8	- 121.8	- 141.8	- 161.6	- 179.6
± 6	- 63.43	- 83.44	- 103.4	- 123.4	- 143.4	- 163.1	- 181.2
± 7	- 64.74	- 84.75	- 104.7	- 124.7	- 144.7	- 164.5	- 182.5
± 8	- 65.87	- 85.87	- 105.8	- 125.8	- 145.8	- 165.6	- 183.6

Table 2 K_n (dB) with $P = 1 - 10^{-6}$ and N from 10 to 120

N	10	20	40	60	80	100	120
$n - N$							
± 1	- 99.96	- 93.97	- 87.95	- 84.43	- 81.93	- 79.99	- 78.41
± 2	- 105.8	- 99.96	- 93.97	- 90.45	- 87.95	- 86.01	- 84.43
± 3	- 109.2	- 103.4	- 97.48	- 93.97	- 91.47	- 89.53	- 87.95
± 4	- 111.4	- 105.8	- 99.96	- 96.46	- 93.97	- 92.03	- 90.45
± 5	- 113.0	- 107.7	- 101.8	- 98.39	- 95.90	- 93.97	- 92.38
± 6	- 114.2	- 109.2	- 103.4	- 99.96	- 97.48	- 95.54	- 93.97
± 7	- 115.0	- 110.4	- 104.7	- 101.2	- 98.81	- 96.88	- 95.30
± 8	- 115.6	- 111.4	- 105.8	- 102.4	- 99.96	- 98.03	- 96.46

From Table 1, one can observe that K_n reduces nearly 20dB as the $\frac{\Delta t'}{T_{\text{ref}}}$ decreases 10% for the same N , which means the lower the $\frac{\Delta t'}{T_{\text{ref}}}$ is, the lower each order spurious tone is. Minimizing the $\frac{\Delta t'}{T_{\text{ref}}}$ is very essential to the design of a high quality charge pump DLL-based oscillator. It is also a challenge to accomplish a charge pump, especially to CMOS processes for their long transition time and processing divergences. To lower the $\Delta t'$ and lengthen the T_{ref} can meet this challenge. Practically, a $\frac{\Delta t'}{T_{\text{ref}}}$ less than 10^{-5} is required in general specifications for an oscillator with the SFDR (Spurious-Free Dynamic Range) larger than 60dB in transceivers used in mobile communications. For example, to $f_{\text{ref}} = 25\text{MHz}$ and $N = 40$, however, 0.4ps phase error is permitted and it is hard with CMOS implementations refer to the following analysis. Table 2 discloses a simple conclusion, the effect of N on K_n is not as much as that of $\frac{\Delta t'}{T_{\text{ref}}}$, and the dependence of K_n on the N decreases when the N becomes larger. There is relatively relax settlement in the choice of N , the focus to reduce the spurious tones should be more on P than on N .

3 Approaches to Reduce Mismatch

As the analysis above, a very small phase error produces significant spurious tones around the carrier by the reference. To reduce the spurious tones, Eq. (2) gives us following suggestions. Firstly, reduce the Δt as little as possible. The smallest Δt depends on the gate capacitance of the switching MOS transistors when the currents in the charge pumps are large, because of large transistors needed; But when the currents are little, the relatively small capacitance of the small transistors needed makes the switching quickly, the smallest Δt depends the Phase Detector (PD) followed by the charge pump, in which the D flip-flops take at least two or three gate delays (in general, several hun-

dreds of ps) to be reset. Secondly, the mismatch between the current sources of I_1 and I_2 is another factor influencing on the phase error in Eq. (2) which is always the main reason resulting in the $\Delta t'$. Because the Δt is at least several hundreds of ps in value, what we can do turns to the ratio of I_1 and I_2 . Because the switches in the charge pump are implemented with PMOS and NMOS transistors, even the precisely calculated W/L can not agree well with the test results no matter how correct the simulations are. The variances of the CMOS processes and the parameter errors in the MOS transistor models offered by foundries are all the contributors to the current mismatch in a CMOS charge pump. Excellent circuitry topologies are needed here to overcome the difficulties.

An example here describes the challenge for a charge pump with current mismatch for a DLL-based RF oscillator design. Assuming that $T_{\text{ref}} = 40\text{ns}$, $N = 40$ and the carrier will be 1GHz. If the mismatch of I_1 and I_2 is 1% and the Δt is 400ps, which is the sum of the time intervals of one AND and one D flip-flop (this is the general time interval generated by PD^[4]). Then the $\Delta t'$ by Eq. (2) is 4ps and $P = 1 - \frac{\Delta t'}{T_{\text{ref}}} = 1 - \frac{4 \times 10^{-3}}{40} = 0.9999$, in Table 1, this amount of mismatch produces a maximum spurious tone up to -47.92dB. When the LO is integrated in a CMOS transceiver, there is no LC band-pass filter with high Q , this spurious tone will make the transceiver a great degradation in SNR (Signal to Noise Ratio). A phase error about 4ps is reaching the limitation of a CMOS charge pump. One effect way to reduce the spurious tones is to rising the ω_{ref} and a LC tank in CMOS with low Q is quality enough to suppress the spurious tones^[2].

4 Conclusions

A research on the current mismatch in a charge pump is performed. Current mismatch results in a phase error to charge pump DLLs. This phase error is proportional to the mismatch and the

time interval needed to eliminate the “dead zone”. To a selected CMOS process, the current mismatch cannot be improved and a good option to reduce the spurious tones around the carrier by the input reference is to select a PD with the tiniest Δt and low reference frequency. As far as N is concerned, it is not difficult in the design compromises, but low N still expects low spurious tones. The Eq. (11) offers the K_n , the strength of spurious tones, which can be used in the estimation of the performance damage. The example illustrated above discloses the fact that the spurious tone performance of a charge pump DLL-based RF CMOS oscillator can not be superior to a PLL-based one, but because of the good jitter performance and more relax trade-offs of a DLL, and when the input reference is at a relatively high frequency the spurious tones can be suppressed by a LC-tank (integrating high Q inductors is an active field in CMOS processes today), the DLL-based RF CMOS oscillator has a bright future in the design of monolithic RF CMOS

transceivers for mobile communication.

References

- [1] A. Abidi *et al.*, The Future of CMOS Wireless Transceivers, Digest of Technical Papers, International Solid-State Circuit Conference, 1997, 118—119.
- [2] George Chien and Paul R. Gray, A 900-MHz Local Oscillator Using a DLL-Based Frequency Multiplier Technique for PCS Applications, International Solid-State Circuits Conference, San Francisco, CA. Feb. 8, 2000.
- [3] Zheng Junli, Yang Weili and Ying Qiyan, Signal and System (I), Beijing: Higher Education Press, 1991[郑君里, 杨为理, 应启衍编, 信号与系统(上册), 北京: 高等教育出版社, 1991].
- [4] Behzad Razavi, Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits—A Tutorial, IEEE PRESS, Monolithic Phase-Locked Loops And Clock Recovery Circuits' Theory And Design, 1996.
- [5] Beomsup Kim, Todd C. Weigandt and Paul R. Gray, PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, ISCAS, June 1994.
- [6] F. M. Gardner, Charge-Pump Phase-Locked Loops, IEEE Transactions on Communications, 1980, COM-28: 1849—1858.

基于 DLL 的 RF CMOS 振荡器中电荷泵电流源失配

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摘要: 研究了电荷泵中电流源失配造成的假频分量, 推导出了一个用于计算假频分量的公式. 提供了两个数表用于直观了解参数改变时假频变化情况. 最后对设计基于 DLL 的 RF CMOS 振荡器提供了一些参考方法.

关键词: 假频; PLL; DLL; 射频 CMOS 收发器; 本振

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