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A Practical Backside Technology for Indium Phosphide MMICs

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Abstract: A wet etching process for backside via holes suitable for use on InP MMICs technologies is developed for indium phosphide substrate. PMMA is used to mount InP wafer onto glass carrier. Spattered Ta film is utilized as etch mask. HCl+ H_3PO_4 solution realised a etch until a depth of 100μm. It is demonstrated that the wet etching backside process is controllable with large latitudes.

Key words: indium phosphide; MMICs; backside process
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1 Introduction

The fabrication of through-wafer via holes is an essential step in making InP MMICs and the through-via provides a low inductance path between the front side source electrodes and the backside grounding plate. Typically, the substrate is lapped and polished to a thickness of 80—100μm. Although various wet etching and dry etching via holes have been developed for InP[1—3], difficulties still exist as InP substrate is more fragile than GaAs one and the temperature of dry plasma etching of InP must be higher than that of GaAs[4]. Therefore choosing the suitable mounting carrier and suitable mounting glue becomes very important.

Some solid glues like wax have been utilized to mount InP wafer[1]. With a solid glue, it is difficult to control the bake temperature and the bake time, so the wafer is easily broken and air bridge structures on the front side are easily damaged. The dry etching of InP allows to obtain via holes with almost vertical profile[1,2], but the etching temperature is more than 130℃, the etching time is longer than that of wet etching. The wet technique provides another way to achieve InP backside process[3,4]. The key is the adhesion of etch mask to InP substrate which determines the etched profile, the dimension and the yield of via holes and the tolerance of process.

This study supplied a practical method for backside process of indium phosphide MMICs. The glass carrier was chosen, it has an efficient of thermal expansion similar to that of InP and it is transparent, so the mounting quality can be easily controlled. Liquid PMMA solution was used to mount InP wafer. By controlling the temperature, time and thickness of PMMA, it can avoid the break of InP wafers, the damage of air bridge, and at same time obtain even PMMA distribution and more uniform result. PMMA is also easily removed with the solvate after finishing the backside process.

A RIE etched Ta mask was developed. The Ta

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film was spattered at low temperature, resistant to H_3PO_4 and HCl, and easily removed by dry plasma etching. With a Ta mask, the etched profile in InP is not sensitive to solutions and etching times——it is very important for thinned wafers with a difference of thickness (up to 10μm). By the way, Ta can be also used as dry etch mask for chlorine based processes.

This method is controllable with large latitudes.

2 Etch Process

A 50mm InP wafer was mounted upside-down with PMMA on a 75mm glass plate, the thickness of PMMA was approximately 3—4μm. A bake with a temperature of 150℃ and a time of one hour permitted to obtain a sufficient adhesion between wafer and carrier. Then the wafer was chemo-mechanically or abrasively polished to 80—100μm without break. A chemical etching with HCl : H_3PO_4= 1 : 10 was applied to eliminate the surface damage, the etching depth was 5μm. A Ta film with a thickness 150—200nm was sputtered. After lithography, the Ta film was etched at a pressure of 3×10^3Pa with a SF_6 plasma.

A H_3PO_4 : HCl= 1 : 2 or pure HCl solution was used to etch via holes. The etching temperature was 30℃. Figure 1 shows the result under different masks. Figure 1 (a) is obtained with AZ4620 photoresist etched mask. The original mask size is 100μm × 100μm, and the depth of hole is 50μm. After etched, the top dimension of hole in Fig. 1(a) is 280μm × 190μm. This means a graver lateral etching. Figure 1(b) is obtained with the Ta etched mask, the origical mask size of hole is 190μm × 100μm. Along $(1\bar{1}0)$ the lateral etching is only 20μm (10μm each side), and along (110) direction, there is no lateral etching. After etched, the top dimension of hole becomes 190μm×120μm, the depth of hole is 84μm.

With a Ta etched mask, under different etching temperature, solution or different etching

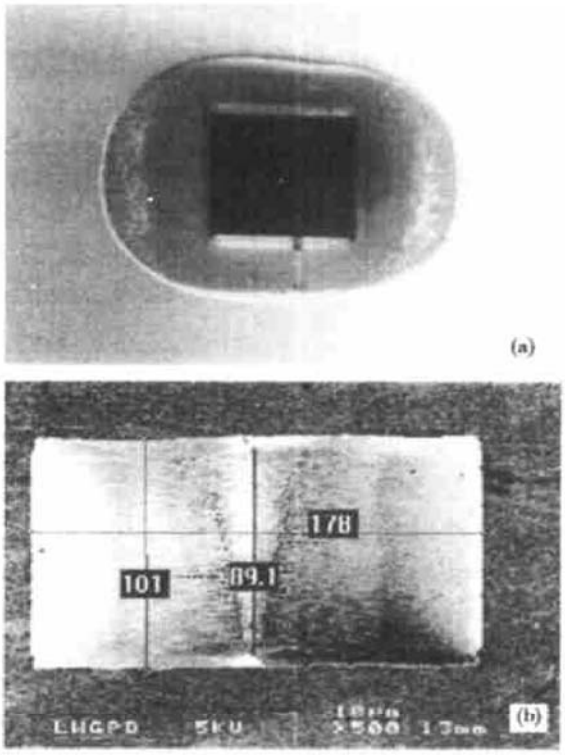

FIG. 1 Etch Results with Different Masks (a) Etch with a AZ4620 Photoresist Mask; (b) Etch with a Ta Mask

times, a stable dimension of via hole was obtained. It demonstrated that with the Ta mask, the via hole geometry with great tolerance to over-etching is achivekle.

Figure 2 is the sections of Fig. 1(b). Along $(1\bar{1}0)$, the etched sidewalls are almost vertical, and along (110), the etched angles is approximately 100° (Fig. 3 and Fig. 6).

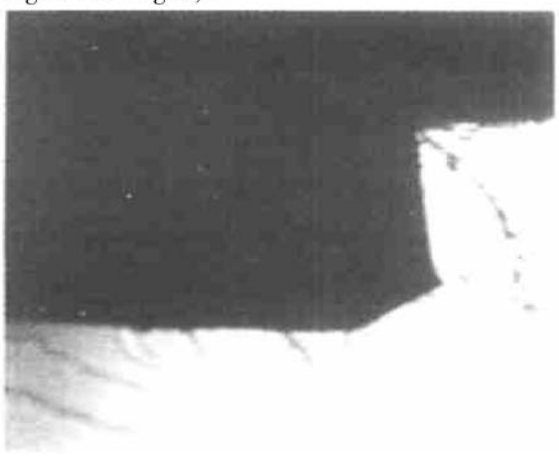

FIG. 2 Section of Via Along $(1\bar{1}0)$

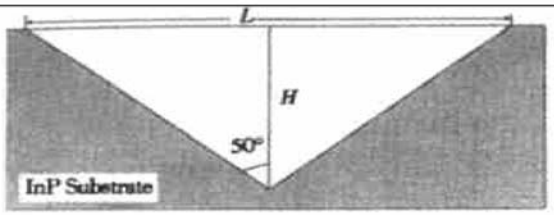

FIG. 3 Etched Angle of Via Hole

In order to obtain via hole with a determined depth H, we must design a mask size of via hole on the basis of formula

$$L = 2H\tan\alpha/2$$

where α is the etched angle(100°), L is the mask width of hole along (110). Figure 4 shows the etched depths as a function of mask sizes along (110).

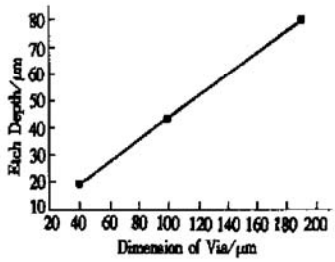

FIG. 4 Etched Depths as Function of Origical Mask Sizes

Figure 5 shows the etching depth as a function of the etching time with a Ta mask. The original mask size is 190μm×100μm, and the etching temperature is 30℃ with the solutions H_3PO_4 : HCl= 1 : 2 and pure HCl respectively. After finishing the depth of 80μm, the etching process almost stoped. It further demonstrated that Ta etched mask made the wafer be able to withstand longer time(twice more than normal etching) with little lateral etching.

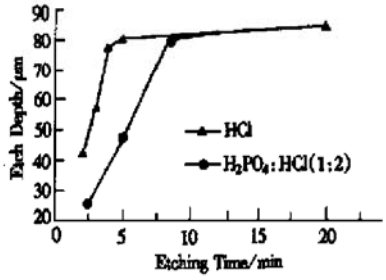

FIG. 5 Etched Depths as Function of Etch Time

3 Metal Deposition

Figure 6 shows the etching profile of via hole. The slopes along (110) direction are smooth, suitable for a deposition of metal films. After the etching of via holes, the Ta film was removed by dry plasma etching. A 250nm NiCr/Au was sputtered, and 4μm Au was plated. Figure 7 shows a part of via holes across 50mm InP thinned to 95μm. The dimension of hole on backside and on frontside is 280μm×80μm and 70μm×70μm respectively.

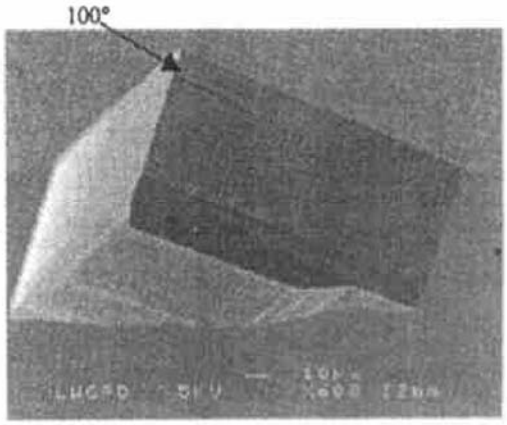

FIG. 6 Etching Profile of Via Hole

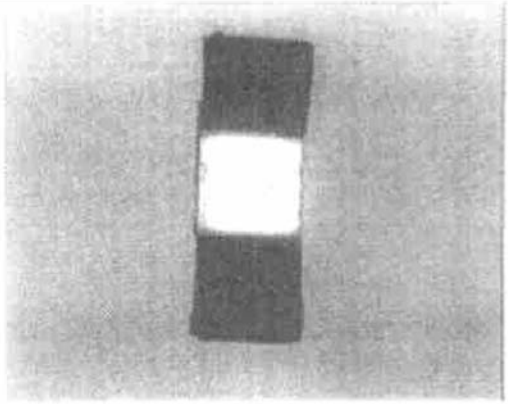

FIG. 7 Picture of Via Hole

4 Conclusion

A backside via hole process suitable for use on monolithic microvave integrated circuit technologies has been developed for indium phosphide, based on the isotropic etching resistance of InP to

some acids. The choice of suitable baking condition of PMMA glue can avoid the crack of thinned InP wafer. The use of Ta film as etching mask greatly increases the process latitude of wet chemistry via holes etching. At the end, the hole with a depth of 100μm has been realised.

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References

[1] R. Khare, J. Brown, M. Hu, D. Pierson, M. Melendes and C. Constantine, J. Vac. Sci. Technol. B, 1994, **12**(5): 2947.

[2] Katerina Y. Hur, Rebecca A. McTaggart and Thomas E. Kazior, 1994 GaAs IC Symposium.

[3] R. Khare, E. L. Hu, J. J. Brown and M. A. Melendes, Proceedings of InP and Related Materials, 1993.

[4] S. Bui, A. Oki, N. Nguyen, L. Tran and D. Streit, Proceedings of InP and Related Materials, 1992.

一种实用的磷化铟MMIC背面工艺技术

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摘要: 采用湿法技术发展了磷化铟MMIC的背面通孔刻蚀工艺, PMMA用作粘片剂, InP衬底粘附于玻璃版上, 溅射钽膜用作湿法刻蚀掩膜, HCl+ H_3PO_4 腐蚀液实现100μm的通孔腐蚀. 已证实这种湿法通孔工艺宽容度大, 精确可控.

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