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Simulation and Design Optimization of Novel Microelectromechanical Digital-to-Analog Converter*

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Abstract: A microelectromechanical Digital-to-Analog Converter (DAC) based on Weighted-Gap (WG) principle is described, which is analogous to the weighed-resistor DAC in electronic circuits. To convert the input of binary voltage to the output of analog displacement, the gaps are proposed to be employed as a scale factor. A finite element method is used to simulate the performance of the DAC. To reduce the error, the structure design is optimized and the maximum error of 0.002μm is obtained.

Key words: digital-to-analog converter; MEMS; microactuators; precise positioning; FEA

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1 Introduction

Traditional actuators are generally driven by analog voltages. One of the main disadvantages of the actuators is that an accurate driving voltage is very environment-prone and difficult to acquire. Microelectromechanical Digital-to-Analog Converter (MEMDAC) is a new approach to accurately control the output of microactuators by using digital signals.

Two prototypes of MEMDAC have been demonstrated by Yeh[1] and Toshiyoshi[2,3]. In Yeh's mechanism, the cascading lever arms and thermal actuator arrays are driven by the voltage of 5V, which is compatible with IC voltage[1]. The nonlinear error caused by the finite translation spring constant at the input beams is 0.3μm, about 5% of the maximum displacement. The MEMDAC provided by Toshiyoshi possesses a comparatively small error about 0.034μm. However, the driving voltage of 150V limits its applications[2,3].

A MEMDAC based on Weighted-Gap (WG) principle, i.e., Weighted-Gap Digital-to-Analog Converter (WGDAC), is presented in this article. The actuators in the WGDAC are driven by a 5V voltage. The structure is simulated by ANSYS. The error of WGDAC is proved no more than 0.002μm. 2^N kinds of displacements can be obtained by using an N-bit binary signal.

2 Principle

A WGDAC proposed here is a mechanical counterpart of weighted-resistor DAC in electronic circuits and the gaps are utilized as the scale factor instead of the resistance. The sketch of a 4-bit WGDAC is shown in Fig. 1. The lateral displace-

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ment of the output beam on the top is measured to be the analog output of WGDAC. To transport the displacements of the actuators to the output beam, 4 lateral beams are used that are narrower than the output beam. The 4 lateral beams are connected to the output beam so that the D/A converting can be implemented.

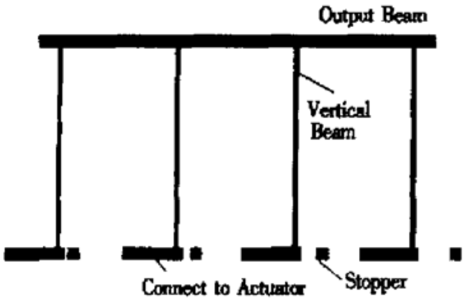

FIG. 1 Diagram of a 4-bit WGDAC

A segment of the WGDAC is shown in Fig. 2, with thermal actuator arrays acting as input units and the binary 5V signal applied[4,5]. If the input signal B_i is "0" on this bit, no voltage will be applied to the actuators, and the array will keep still with the lateral beam. Under "1" signal, the array will be deflected right until the lateral beam touches the stopper. The displacement ranges of N bits are X, $2X$, ……, $2^{N-1}X$, where X and $2^{N-1}X$ are the gaps of LSB (Least Significant Bit) and MSB (Most Significant Bit). The ideal result of output is given by: $\text{Output} = \frac{X}{N}\sum_{i=0}^{N-1} 2^i B_i$

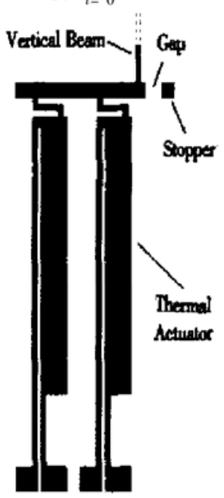

FIG. 2 Input Unit

3 Simulation

Using FEA software ANSYS, we investigate the model of a 4-bit WGDAC. The gaps for LSB and MSB are 1μm and 8μm, respectively. The ideal displacement of the output beam and the error resulted from ANSYS simulation are plotted in Fig. 3. By applying the input of "1100", the maximum error is obtained to be 0.09μm. As a result, this DAC could hardly be extended to more bits.

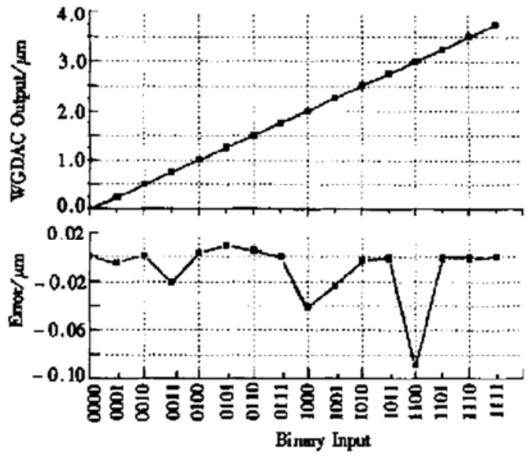

FIG. 3 Ideal Output and Error

Several factors are found to cause the error. The displacement of a thermal actuator has both useful lateral component and harmful vertical displacement, which is the main reason of the error. In addition, the flexure of the vertical beams is not completely linear, and the output beam is not absolutely rigid, either.

4 Optimization

According to the results obtained above, we have modified the original WGDAC design. As shown in Fig. 4, the asymmetric structure is replaced by a symmetric one that includes 8 vertical beams and arrays. The width of the output beam is broadened from 6μm to 12μm. In order to reduce the error induced by the vertical displacement, the sequence of the input 4-bit signal is rearranged as "B_0, B_4, B_2, B_1" instead of "B_0, B_1, B_2, B_3".

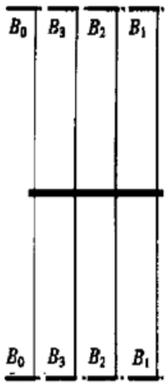

FIG.4　Optimized Structure

The optimized WGDAC is analyzed and the maximum error is 0.002μm, much smaller than that in Yeh's and Toshiyoshi's model[1,2]. The errors of 2^4 inputs are shown in Table 1. This DAC can be extended to 8 bits. The dynamic responses of the WGDAC and the WGDAC driven by electrostatic actuators are still under investigation. Detailed results will be reported elsewhere.

Table 1　Errors of Optimized WGDAC

Input	0000	0001	0010	0011	0100	0101	0110	0111
Error/μm	0.000	0.000	0.000	0.000	0.000	0.000	0.002	0.000
Input	1000	1001	1010	1011	1100	1101	1110	1111
Error/μm	0.001	0.001	0.001	0.001	0.002	0.002	0.002	0.002

5　Conclusion

We have demonstrated, for the first time, a weighted-gap DAC. The finite element analysis has proved the precise location of the output beam. This DAC can find wide applications in micromirror, fiber-optic switch, STM probe, and data storage system.

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一种新颖微机械数模转换器的模拟与设计优化*

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摘要: 提出了一种基于权间隙原理的微机械数模转换器(WGDAC), 它与电路中的权电阻数模转换器的原理类似, 利用间隙的长度作为比例因子, 从而实现由二进制电压输入到模拟位移输出的转换. 给出了有限元方法分析对由热执行器阵列驱动的数模转换器的输出位移分析的结果. 为了减小误差, 对结构作了优化设计, 使误差不大于 0.002μm.

关键词: 数模转换器; 微电子机械系统; 微执行器; 精确定位; 有限元分析

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