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Epitaxial Growth of 150mm Silicon Epi-Wafers for Advanced IC Applications*

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Abstract: With the device feature's size miniaturization in very large scale integrated circuit and ultralarge scale integrated circuit towards the sub-micron and beyond level, the next generation of IC device requires silicon wafers with more improved electrical characteristics and reliability as well as a high perfection of the wafer surface. Compared with the polished wafer with a relatively high density of crystal originated defects (e. g. COPs), silicon epi-wafers can meet such high requirements. The current development of researches on the 150mm silicon epi-wafers for advanced IC applications is described. The P/P^+ CMOS silicon epi-wafers were fabricated on a PE2061 Epitaxial Reactor (made by Italian LPE Company). The material parameters of epi-wafers, such as epi-defects, uniformity of thickness and resistivity, transition width, and minority carrier generation lifetime for epi-layer were characterized in detail. It is demonstrated that the 150mm silicon epi-wafers on PE2061 can meet the stringent requirements for the advanced IC applications.

Key words: silicon; epitaxial growth
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用于先进 CMOS 电路的 150mm 硅外延片外延生长*

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摘要: 随着大规模和超大规模集成电路特征尺寸向亚微米、深亚微米发展, 下一代集成电路对硅片的表面晶体完整性和电学性能提出了更高的要求. 与含有高密度晶体原生缺陷的硅抛光片相比, 硅外延片一般能满足这些要求. 该文报道了应用于先进集成电路的 150mm P/P^+ CMOS 硅外

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延片研究进展. 在 PE2061 硅外延炉上进行了 P/P^+ 硅外延生长. 外延片特征参数, 如外延层厚度、电阻率均匀性, 过渡区宽度及少子产生寿命进行了详细表征. 研究表明: 150mm P/P^+ CMOS 硅外延片能够满足先进集成电路对材料更高要求,

关键词: 硅; 外延生长
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1 Introduction

With the continued scaling of device structures to the micron and sub-micron levels, the application of epitaxial wafers for the advanced CMOS VLSI technology becomes more widespread[1—3]. P/P^+ and N/N^+ epitaxial structures have been demonstrated how to offer the inherent advantages as starting materials over the bulk substrates: reduction of latch-up susceptibility[4]; improvement of radiation hardness; free of crystal originated defects (COPs) on the surface region near the device's active layer, therefore the higher gate oxide integrity (GOI) yields. In order to meet the stringent requirements of sub-micron or beyond the design-rule devices, the epitaxial wafer quality, especially the structural characteristics of silicon epitaxial layers, should be further improved. Although low-temperature epitaxy techniques, such as MBE and UHV/CVD[5], have been developed in recent year, atmosphere-pressure CVD process is widely applied in the epitaxial silicon wafer production.

Three decades ago, the researches on the epitaxial silicon materials began in China, which were focus on the epi-wafer with diameter of 75mm or smaller. Recently, some key microelectronic projects have been launched. These projects are designed to produce 0.35 micron IC chips. The importance attaches to the development of epitaxial silicon materials with large diameter of 150mm or above. The main aim of our recent project is to research into the epitaxial growth of P/P^+ or N/N^+ silicon epi-wafers with the diameter of 150mm and to provide the edge technology for the production of large-diameter silicon epitaxial materials.

In this work, we report on the initial development of epitaxial growth of large diameter silicon epi-wafers on the newly-introduced epitaxial reactor PE 2061. In particular, some latest results of 150mm P/P^+ CMOS silicon epi-wafers are demonstrated in detail. Those material parameters include epi-defects, uniformity of thickness and resistivity, transition width, and minority carrier generation lifetime. The result of device fabrication by using the materials will be discussed in another article.

2 Epitaxial Reactor and Growth Conditions

The epitaxial reactor PE2061 was manufactured by Italian LPE Company. This new

model reactor was first introduced into China in late 1998. Its main features include: (a) twin chamber concept with large batch load (see Table 1) and short circle time; (b) 4kHz solid state low frequency induction heating system; (c) strong compatibility for wafer diameter (up to 200mm) and epi-layer thickness (up to 100μm); (d) undoped resistivity above 500 Ω·cm.

Table 1 Loading Capacity Per Chamber

100mm	30 wafers
125mm	24 wafers
150mm	14 wafers
200mm	5 wafers

The 150mm P/P^+ and intrinsic silicon epi-wafers were grown in hydrogen ambients at the temperature of 1120℃. The main hydrogen flow rate was 300 l/min. The liquid $SiHCl_3$ was used as silicon source with flow rate being 35 g/min. The doping gases were B_2H_6 and PH_3. The substrates were heavily doped N or P type silicon wafers. In order to implement the extrinsic gettering and control the autodoping from the heavily-doped silicon substrate, the backside of the epitaxial substrate were sealed with poly silicon of 1.2μm and low-temperature silicon oxide layer of 350 nm. HCl gas etching at 4l/min flow rate was carried out at the temperature 1130℃ for 6 minutes before epitaxial deposition. The epitaxial growth rate was nearly 1μm/min. The silicon epi-wafers were characterized in detail by electrical measurements such as Spreading Resistivity Probe (SRP), MOS Capacitance-time (C-t) technique. The epilayer thickness is measured with the infrared reflect method.

3 Results and Discussion

3.1 <100> I/N^+ Intrinsic Epilayers

Undoped intrinsic silicon epilayer quality, in particular, intrinsic resistivity value reflects the cleanness or contamination level of the whole epitaxial reactor, including susceptor, bell-jar, gas pipeline and gas distribution system, and the purity of doping gas and liquid silicon source. The intrinsic silicon epilayer was grown without intentionally doping on the 100mm n-type heavily-doped silicon substrate. The epilayer thickness was 45μm. The intrinsic epilayer was found to be n-type. The dopant transition region of intrinsic layer is very abrupt and the transition width is less than 1 micron (see Table 2). In our experiment, the guaranteed intrinsic resistivity is more than 500Ω·cm. The typical value is 700Ω·cm. The maximum is up to 1000 Ω·cm. The carrier generation lifetime of intrinsic layer was measured to be more than 10, 000 microseconds. This parameter also indicates that the high value of intrinsic resistivity is not due to the impurity compensation. The result on intrinsic layer confirms that the epitaxial reactor system has high cleanness.

Table 2 Typical Parameters of I/N^+ Intrinsic Layer

thickness	resistivity	lifetime	trans. width
45μm	700Ω·cm	> 10ms	< 1μm

3.2 150mm <100> P/P^+ Silicon Epi-Wafers

P-type epilayer was grown on 150mm < 100> heavily B-doped back-sealed silicon substrate. The P/P^+ epiwafers was supplied to fabricate the advanced CMOS devices. The resistivity and minority carrier generation lifetime of epilayers were measured by spreading resistivity probe and MOS C-t technique respectively. The stacking faults and dislocations were detected by the chemical etching and microscopy method. Figure 1 shows the typical depth profile of spreading resistivity. From the profile, the transition width was obtained. Table 3 summaries the five-point thickness, resistivity and transition width data within one wafer. The thickness and resistivity variations of the epiwafer are less than 0.3% and 5% (see Table 3). The 5-point thickness and resistivity data show that the epiwafer exhibits an excellent thickness and resistivity uniformity across the whole wafer. From Fig. 1, it is seen that the transition region of epilayer for P/P^+ structure is very abrupt and the dopant transition width is less than 1 micron. The 5-point generation lifetime vasies with the specified locations on the surface. It implies that the variation of lifetime might result from the nonuniform distribution of oxygen precipitation and heavy metal impurity contamination. Therefore, it is of importance to control the oxygen uniform distribution and the oxygen precipitation in order to implement the efficient internal gettering in the epi-substrate to improve the epilayer quality, especially, the generation lifetime parameter.

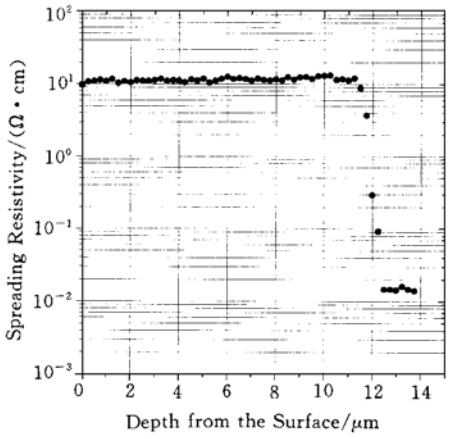

FIG. 1　Typical Depth Profile of Spreading Resistivity for 150mm < 100> P/P+ Epiwafers

Table 3　Typical Parameters of P/P^+ < 100> Silicon Epi-Wafers

Parameters	1	2	3	4	5	Uniformity
Thickness/μm	11.97	11.96	12.04	11.98	11.99	≤0.3%
Resistivity/(Ω·cm)	10.9	11.5	12.1	11.82	11.49	≤5%
Transition Width/μm	< 1	< 1	< 1	< 1	< 1	
Lifetime/μs	103	289	155	143	98	
Stacking Faults/cm^{-2}	None					
Dislocations/(/wafer)	None					
Light Point Defects (0.16μm to 5.12μm)/wafer	< 20					

Besides the thickness, resistivity and lifetime parameters, the stacking faults and dislocations are also listed in Table 3. In our measurement, no stacking faults and dislocations were observed across the whole wafer. But the particles or light point defects

on the surface were detected. The total particles with the size ranging between 0.16μm and 5.12μm, across the wafer were less than 20 per wafer. Those basic material parameters of 150mm P/P^+ epiwafers confirm that the 150mm epiwafers, which grown on PE2061 reactor in our laboratory have excellent crystalline perfection and can meet the requirements of sub-micron or beyond design rule IC devices. The detailed device parameters will be discussed in later paper.

4 Summary

150mm silicon epiwafers were fabricated on PE2061 at the Northern Microelectronic R & D Center based in Beijing. The P/P^+ CMOS epiwafers have an excellent thickness and resistivity uniformity, abrupt transition region and higher minority carrier generation lifetime. In addition, the silicon epiwafers have good crystalline perfection: free of stacking faults and dislocations and low surface light points defects. It demonstrate that the silicon epiwafers can meet the requirements of the sub-micron and beyond design-rule CMOS devices.

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