第 21 卷第 9 期　　半　导　体　学　报　　Vol. 21, No. 9
2000 年 9 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Sep., 2000

Novel Oxide Trap Behavior in Ultra Thin Gate and Its Study by PDO Method

WANG Zi-ou(王子欧), MAO Ling-feng(毛凌峰), WEI Jian-lin(卫建林), XU Ming-zhen(许铭真) and TAN Chang-hua(谭长华)

(*Institute of Microelectronics, Peking University, Beijing* 100871, *China*)

Abstract: The degradation of MOSFETs under high field stress has been investigated for a long time. The degradation is due to the newly generated traps. As the gate thickness scaled down rapidly, a conventional method for detecting oxide traps, such as *C-V* or subthreshold swing, is no longer effective. Some new phenomena also appear, such as Stress Induced Leakage Current (SILC) and soft-breakdown. The oxide traps' behavior and their characteristics are the key problems in the study of degradation. By extracting the change of transition coefficients from the *I-V* curve and using the PDO (Proportional Differential Operator) method, various oxide traps can be distinguished and as would be helpful in the determination of trap behavior changes during the degradation process.

Key words: relative transition coefficient; SILC

PACC: 7755

CLC Number: O472　**Document code**: A　**Article ID**: 0253-4177(2000)09-0857-05

1 Introduction

Oxide traps for stressed MOSFET's have been extensively investigated in the past decades, and the trap generation mechanism was presented[1—4]. When oxide film is thinner than approximately 7nm, some new phenomena, such as SILC and soft-breakdown, will appear under a high field stress. It is widely accepted that these phenomena are closely related to the oxide traps formed during degradation. The

WANG Zi-ou (王子欧) received his BS degree in Physics in 1991 and MS degree in electronics in 1997 from Dalian University of Technology. Now he is pursuing the doctor degree in Peking University. His current research is on the reliability and physics of deep submicron devices.

XU Ming-zhen (许铭真) is now a professor in the Department of Computer Science and Technology, Peking University. Her research activities include the electrical characterization and reliability of MOSFETs with thin gate dielectric, Si/SiO_2 interface physics, high field physics and breakdown mechanism, and modeling of MOS devices.

TAN Chang-hua (谭长华) is now a professor in the Department of Computer Science and Technology, Peking University. His research interests include small scale MOS device physics, Si/SiO_2 interface physics, degradation mechanism of MOS device.

Received 31 January 2000, revised manuscript received 27 April 2000

distribution and the characteristic of the oxide traps, however, are still not clear. In this letter, by measuring the transient I–V characteristic after stressing and by studying the change of transition coefficients with stress time and gate voltage, the localized energy levels of oxide traps and their position could be defined. By PDO method, the trap's character could be described by a time concerned parameter.

2 Experiment

The samples in experiments are N-MOSFETs with thin gate oxide thickness of 5nm and thick gate oxide thickness of 7nm, gate area 15μm×15.025μm, and with a n^+ poly-Si gate. Samples are applied to the positive 6.1V constant voltage when the source, drain, and the substrate are grounded at the temperature of 300K. After every cycle of the stress, the I–V measurements are performed. The measurement time can be neglected compared with the stress time. All of the samples are stressed till breakdown. All experiments are conducted by a HP4145B with a PC controller automatically acquiring data.

3 Results and Analysis

We define the relative transition coefficient as $T = J(t)/J(0)$ at different gate voltages V_{ox}. Here $J(0)$ is the initial gate current density before the stress is applied, and $J(t)$ is the gate current density during the degradation process before breakdown. Figure 1 shows T as a function of the stress time t when the measurement voltage between 4.3—6.1V with a step of 0.2V. Figure 2 shows the relation between T and the measuring voltage, curve a is T just before the breakdown, while curve b is that at the middle time of degradation process. In Figure 1, when the measuring voltage V_{ox} is less than 4.7V, T is higher than 1 and increases monotonically with the stress time t, which is called SILC phenomena[4] under low field, as has been frequently reported, and could be explained as trap assisted tunneling. When V_{ox} is between 4.7V and 5.1V, T decreases monotonically with t, and T interval between different voltage is very large compared with that of V_{ox} higher than 5.1V. Obviously, some localized energy levels have formed. It suggests that the decline of gate current after stress is caused by trapped electrons[5], but the change of

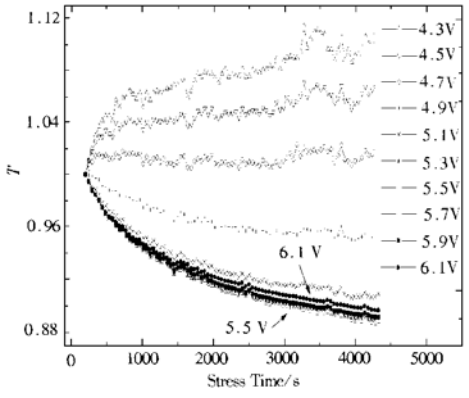

FIG. 1 For 5nm Sample. The relative transition coefficient $T = J(t)/J(0)$–stress time t curves for different measuring voltages before breakdown occurred. For various curves, the measuring voltages are from 4.3V to 5.5V; For various curves lift from bottom, the measuring voltages are from 5.5V to 6.1V; The curve responding to 5.5V is the lowest curve.

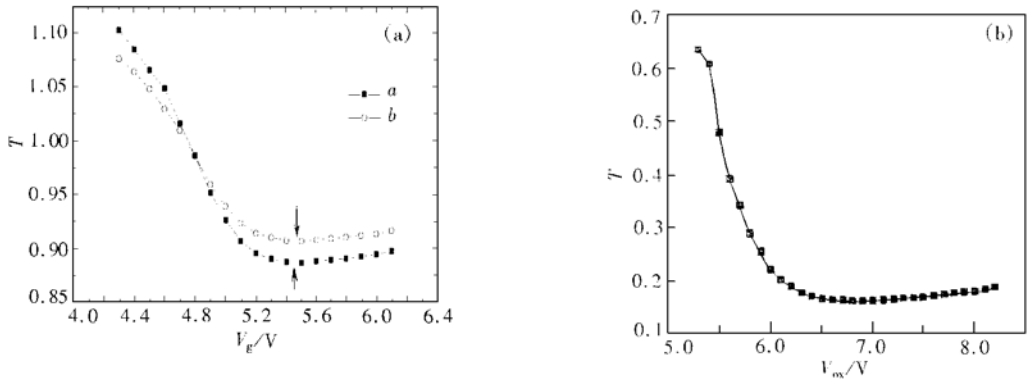

FIG. 2 (a) For 5nm Sample. The relation between the transition coefficient T and with measuring voltage at a certain time, curve a is T just before breakdown, curve b is T in the middle of degradation process. (b) For 7nm Sample Just Before Breakdown.

transition coefficient for different gate voltages is different. The above results could be explained in Fig. 3 (a). E_t stands for the energy levels of oxide traps.

The traps in the gate oxide could be regarded as an effective center at their centroid, and their energy levels continuously distribute down from the conduction band of gate oxide. When injection carrier is at the level lower than the top E_t, these E_t significantly affect the transition coefficient T, making T very different under different measuring voltage. As the corresponding injection level reaches the top E_t, the decline of transition coefficient T becomes more serious because of the oxide traps. When the injection level is higher than the top E_t, the tunneling through the top triangular barrier, as shown in Fig. 3, will dominate the transition coefficient, which leads to a small continuous increase of T. A turning point exists. Figure 2 (a) shows the change of T as a function of measuring voltage V_g for 5nm samples. Curve a stand for T before breakdown occurs, while curve b

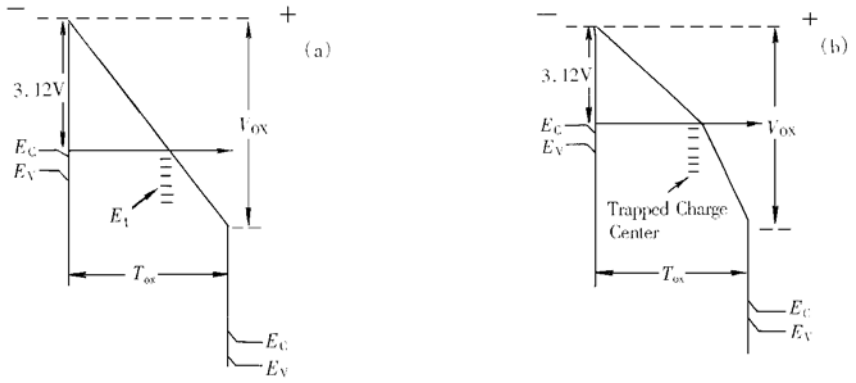

FIG. 3 (a) For 5nm Sample, The localized energy level and the position of the trap centroid, E_t is trap energy level, T_{ox} is the gate thickness, V_{ox} is the voltage applied on the gate oxide, (b) the abrupt electric field model for the turning point

is that in the middle time during the degradation process. When V_{ox} is 5.5V, the injection level is just corresponding to the top E_t. At the turning point, the trap centroid could be directly evaluated using simple triangular barrier calculation. Supposing the distance from the conduction band of oxide film to the conduction band edge at the surface of substrate silicon is 3.12V, $3.12/V_{ox} = x/T_{ox}$, where T_{ox} is the gate oxide thickness, x is the position of the trap centroid and $V_{ox} = 5.5 - \Psi_S - V_{FB}$. The position is approximately 3.8nm from the substrate, which could also be explained by the model in Fig. 3 (b). The turning point corresponds to the abrupt change of electric field caused by the trapped charge.

For samples with the same stress and same temperature, this position is the same. It should be noticed that the same turning point also exists on curve *b* of Fig. 2 (a), as marked by arrows. It clearly shows that such trap centroid has been determined at the early degradation process. In Fig. 1, the curve marked 5.5V is at the lowest position and the curve marked 6.1V is above the curves marked 5.5, 5.7 and 5.9V, which is corresponding to Fig. 2. At the turning point, when the $dT/dV_{OX} = 0$, the emission and capture establish a dynamic balance. When the position of V_{OX} is below this point, the traps capturing ratio will be larger than the emission ratio; when it is at the right side of this point, the situation will be changed. For 7nm samples under the same field stress, the turning point is about 6.75V, which is closer to the cathode. As can be shown by Fig. 2 (b).

From Fig. 2, the dT/dV_{ox} is negative and almost linear when V_{ox} is between 4.7 and 5.5V. When V_{ox} is less than 4.7V, however, another mechanism is dominant and makes T to be greater than 1, namely SILC. There is a point between 4.7V and 4.8V, at which two effects overlap to make T keep around 1 and change little with the stress time. As V_{ox} increases, the SILC effect becomes more and more insignificant. When V_{ox} is larger than 4.8V, T tends to become saturated with time, and the SILC effect will gradually become small. Obviously, the SILC is not the reason for some kinds of deep level traps.

Since the gate currents have a change about 10% only, and the electric field on the gate oxide changes a little, the situation can be approximated by the first order rate equation. When V_{ox} is less than 4.7V or higher than 4.8V, the gate current curves in Fig. 1 show monotonic character and can be simulated by

$$\Delta J(t) = J(t) - J(0) = J_S[1 \pm \exp(-t < \tau >)]$$

where J_S is the positive constant, and τ is the character parameter reflecting the information of traps that take effect and x_0 is related to the capture/generation ratio. The second term of the right side is negative for $V_{ox} > 4.7$V and positive for $V_{ox} < 4.7$V. Obviously, such curves satisfy the character of PDO method that was first proposed and verified by Xu[6,7]. The character parameter $< \tau >$ can be picked up with PDO method for each measuring voltage V_{ox}:

$$T(kt) = J(kt)/J(0)$$

where k is an arbitrary coefficient larger than 1, and

$$\Delta_P T = T(kt) - T(t) = \frac{J_S}{J(0)}(\exp(-kt/<\tau>) \mp \exp(-t/<\tau>))$$

there must be a maximum value t_P, thus the character parameter τ can be acquired by

$$\tau = \frac{\ln k}{k-1} t_P$$

t_P is the peak position. Different τ reflects the information of different types of traps. The PDO result of the curves in Fig. 1 is shown in Fig. 4. In Fig. 4, when V_{ox} is smaller than 4.7V, two types of traps take effect for each curve in Fig. 1. One trap with τ of group a1 only takes effect before 4.7V and might be a main cause of SILC; the τ of group b1 must be of some shallow traps that only takes effect in the high field FN region. The τ of group a2 seems to have some relation with that of curve b2, which may distribute down from the conduction band continually.

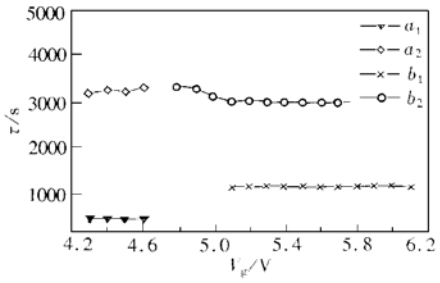

FIG. 4　Different Traps Take Effect of Different V_{ox}

The character parameter τ could be divided into four groups: for measuring voltages less than 4.7V, $a1$, $a2$ take effects; when $V_{ox}>$ 5.1V, $b1$ takes effect; when $V_{ox}>$ 4.8V, $b2$ takes effect.

4 Conclusion

The T-V curves can be divided into four groups. For 5nm samples, when $V_{ox}<$ 4.7V, SILC mechanism dominates the change of T, and it goes on taking effect and gradually declines when $V_{ox}>$ 4.7V. For the second group, when 4.7V $< V_{ox} <$ 5.1V, E_t make a relative big difference on T for different V_{ox}. When $V_{ox}>$ 5.5V, T decreases with time and increases with V_{ox}. This turning point can be used to evaluate the position of electron trap centroid, which has been determined at an early stage of the degradation process. By PDO method, different types of traps can be characterized by different time concerned parameter τ.

Acknowledgement: This work is surpported by Motorola Company, the equipment and samples are also provided by Motorola.

References

[1] Ih-chin CHEN, Stephen E. Holland and Chenming HU, IEEE Trans. ED, 1998, **32**(2): 413—422.

[2] D. A. Buchanan and D. J. Dimaria, J. Appl. Phys., 1990, **67**(12): 7439—7452.

[3] E. HARARI, Appl. Phys. Lett., 1977, **30**: 601.

[4] D. J. Dimaria and E. Cartier, J. Appl. Phys., 1995, **78**(6): 3883—3894.

[5] David J. Dumin, IEEE Trans. ED, 1995, **42**(4): 760—772.

[6] Mingzhen Xu and Changhua Tan, J. Appl. Phys., 1990, **67**(11): 6924—6929.

[7] Mingzhen Xu and Changhua Tan, IEEE Trans. ED, 1996, **439**(4): 628—635.