第 24 卷第 2 期　　半 导 体 学 报　　Vol. 24, No. 2
2003 年 2 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Feb., 2003

Investigation of Thermal Property of Novel DSOI MOSFETs Fabricated with Local SIMOX Technique*

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Abstract: DSOI, bulk-Si and SOI MOSFETs are fabricated on the same die successfully using local oxygen implantation process. The thermal properties of the three kinds of devices are described and compared from simulation and measurement. Both simulation and measurement prove that DSOI MOSFETs have the advantage of much lower thermal resistance of substrate and suffer less severe self-heating effect than their SOI counterparts. At the same time, the electrical advantages of SOI devices can stay. The thermal resistance of DSOI devices is very close to that of bulk devices and DSOI devices can keep this advantage into deep sub-micron realm.

Key words: DSOI; SOI; local SIMOX; self-heating effect; thermal resistance
EEACC: 2530F; 7320R
CLC number: TN386　　**Document code**:　　**Article ID**: 0253-4177(2003)02-0117-05

1 Introduction

Drain and source on insulator (DSOI) structure[1] is proposed to suppress severe self-heating effect and floating body effect in silicon-on-insulator (SOI) devices, which become the main drawbacks of SOI structure. Modern SOI devices have many advantages compared with conventional bulk devices. The existence of buried dioxide reduces parasitic drain and source junction capacitances and fully isolates devices, which facilitates faster circuits and prevents latch up between devices[2]. However, one main drawback of SOI devices is the severe self-heating effect due to low thermal conductivity of buried SiO_2 layer, which is a factor of 100 worse than silicon. Heat generated by the device can not transfer easily from the silicon film to the substrate, so the silicon film may be over hot somewhere, and will cause serious problems in SOI circuits. High temperature will reduce the carrier mobility in the channel so as to degrade the device performance and even make interconnection of the system unreliable. When the silicon film is getting thinner, the self-heating effect is getting more severe[3], so the most promising fully depleted SOI devices, which are fabricated on ultra-thin silicon film, suffer the most severe self-heating effect. This drawback restricts SOI devices to low power applications only. Another main drawback of SOI devices is the floating-body effect (FBE) due to the impact ionization-triggered activation of the parasitic npn bipolar junction transistor in the n-channel SOI MOSFETs. This effect results not only in

* Project supported by National Natural Science Foundation of China (No. 59995550-1) and Special Funds for Major State Basic Research Project (No. G2000036501)

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Received 23 July 2002, revised manuscript received 9 October 2002

loss of gate control but also in severe hot carrier effects (HCE)[4], which is detrimental to the long-term reliability of SOI devices.

A novel DSOI structure[1] is proposed to overcome these drawbacks. With a silicon window below the channel, thermal resistance of substrate is diminished significantly, and floating body effect is totally eliminated because the body regions of DSOI MOSFETs are connected to the substrate. With the development of SIMOX (separation by implantation of oxygen) technique, low dose and low energy implantation has been widely used, which makes it possible to implement DSOI structure by local SIMOX[5] technique with only one additional mask. Bulk-Si, SOI and DSOI MOSFETs are integrated on the same die using this technique. Their thermal resistances of substrate are measured and compared. 2D simulation with Ansys®[6] is also done for deep insight into the heat transport process of DSOI devices and the thermal property in deep sub-micron realm.

2 Fabrication and structure of DSOI MOSFETs

N-channel devices of the three kinds were fabricated on the same die with various channel length. After oxygen implantation ($4.8\times10^{17}cm^{-2}$ at 140keV) with a mask of a 500nm-thick oxide layer above the channel region, the wafer was annealed at 1300℃ for 5h in an Ar/3% O_2 ambient. Buried oxide layer was formed with silicon window below DSOI MOSFETs' channel. Conventional n-MOS process followed oxide implantation to complete the devices. This technique is compatible with bulk-Si and SOI technique. Figure 1 shows the SEM photo of a DSOI MOSFET with W/L equal to 30μm/0.5μm. The well formed buried oxide under drain and source region can be seen clearly. The thickness of silicon film was 120nm; the thickness of buried oxide was 90nm; and the thickness of gate oxide was 20nm.

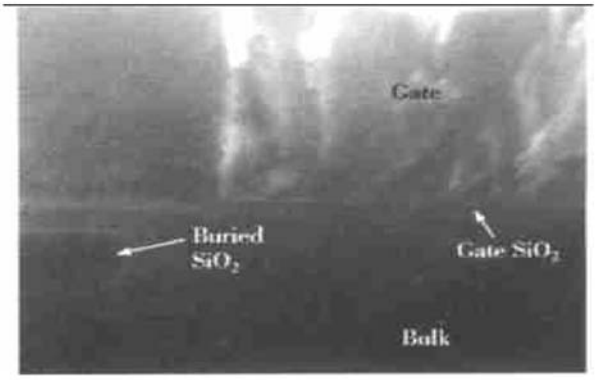

Fig. 1 SEM image of the 30μm/0.5μm DSOI device

3 Measurement of thermal resistance of substrate

Thermal resistance was measured by gate resistance thermometry[7]. The measurements were done on MOSFET structures with four gate contacts as shown in Fig. 2. The gate resistance versus temperature was first measured in the OFF state

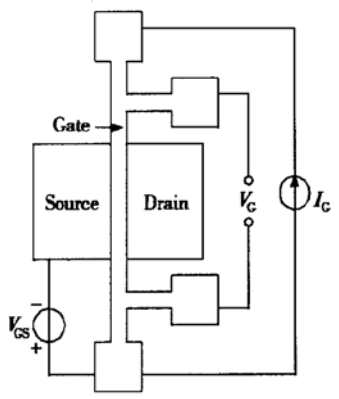

Fig. 2 Bird's-eye test structure of thermal resistance

on a heated plane, and then versus power dissipation when the plane was kept to 300K. When measuring gate resistance versus power dissipation, V_{GS} was set to 6V and V_{DS} was swept from 0V to 6V to change the power generated in the channel. Both the width of silicon windows of DSOI MOSFETs and the length of channel of each device were 0.8μm. The gate resistance versus power dissipation was measured, and then transformed to channel temperature versus power dissipation by the

gate resistance versus channel temperature data measured before. The result is depicted in Fig. 3.

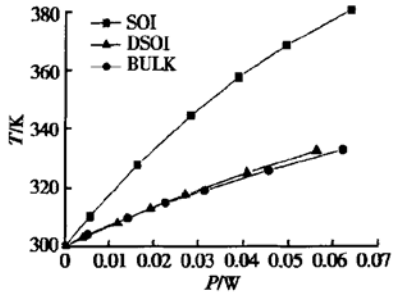

Fig. 3　Measured channel temperature versus power dissipation

Due to the definition of thermal resistance

$$R_{\mathrm{th}} = \frac{\Delta T}{P} = \frac{T_{\mathrm{channel}} - T_{\mathrm{ambi}}}{I_{\mathrm{DS}} V_{\mathrm{DS}}}$$

where T_{channel} is the channel temperature, T_{ambi} is the ambience temperature, and P is the power generated in the channel, which is equal to $I_{\mathrm{DS}} V_{\mathrm{DS}}$, the slope of each curve is in direct ratio with each device's thermal resistance. It is obvious that the thermal resistance of a DSOI device is much lower than that of an SOI device and is nearly equal to that of a bulk one.

It can be seen from Fig. 3 that the measured points deviate from a straight line when power dissipation is high. The reason for this phenomenon is probably that other means of heat transport such as convection and radiation take an important part of total heat transfer and reduce the thermal resistance at high temperature. Further more, because the temperature set on the heated plane at the first step is a little higher than the channel temperature. the value of thermal resistance exacted from the result is a little more than its real value.

4　Simulation of heat transfer of substrate

A simplified 2-D model is built to simulate the thermal transfer of substrate in Ansys®. Because heat transport is dominated by the bulk[8], the influence of heat flow through the metal interconnection is neglected. Figure 4 shows the simplified cross section of a DSOI structure for simulating the thermal resistance. The counterpart of an SOI one is almost the same as it excepted that the silicon window is substituted with oxide. Heat is generated uniformly in the channel region, and 300K boundary condition at the bottom of substrate is used. The values used for default of thermal conductivity are, respectively, 148, 63, and 1.4W/(m·K) for undoped silicon, doped silicon, and buried oxide[9].

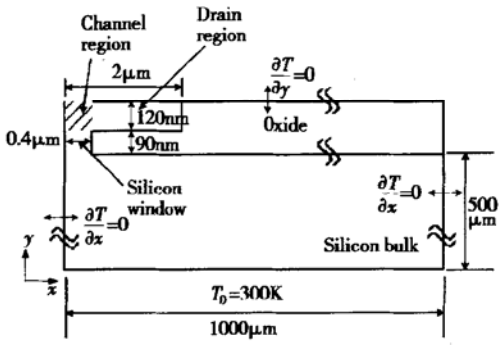

Fig. 4　Simplified cross section of DSOI structure for simulating thermal resistance of substrate

When the power generated in the channel region is 1mW, the 2-D temperature profiles of SOI and DSOI structure are shown as Fig. 5. It can be seen that the temperature gradient in a DSOI MOSFET's buried oxide is much smaller than that in an SOI MOSFET's buried oxide, which indicates that the thermal resistance contributed by buried oxide is reduced significantly in DSOI devices. The silicon window below channel in DSOI device serves very successfully as a path of heat transfer. The peak temperature in the channel of a DSOI device is much lower than that of an SOI device. Their normalized thermal resistances ($R_{\mathrm{th}} W$) extracted from both simulation results and measured results are all listed in Table 1. The simulation results fit with the measured results quite well.

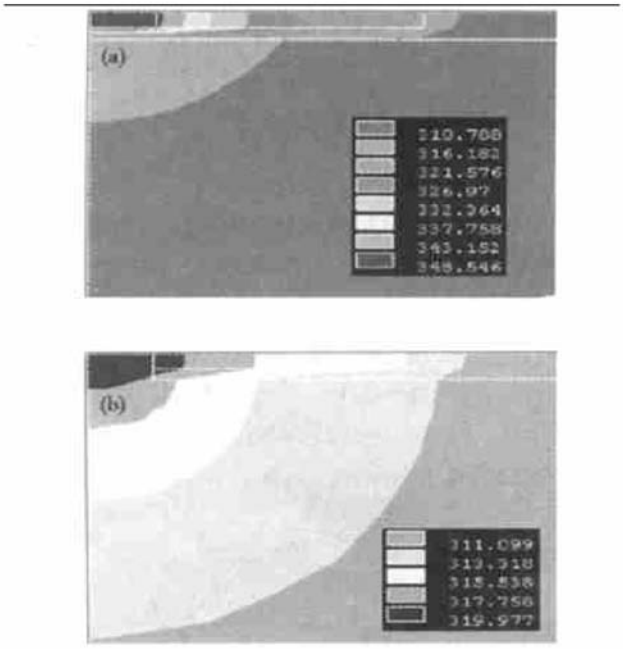

Fig. 5 2-D temperature profile near SOI and DSOI devices when power generation in the channel being 1mW (a) SOI device; (b) DSOI device

Table 1 Normalized thermal resistances extracted from simulation results and measured results Channel length= 0.8μm

Type	Normalized thermal resistance/(K · μm · W^{-1})	
	Simulated	Measured
SOI	49546	47131
DSOI	20997	20047
BULK	20318	19345

Horizontally scaling down the device region and continuing the simulation, an $R_{th}W$ versus channel length diagram is attained in Fig. 6. When the device is getting smaller, the thermal resistance of SOI device increases rapidly, but DSOI device can remain the advantage of smaller thermal resistance. In deep sub-micron realm, DSOI devices still succeed to suppress self-heating effect to the level close to bulk devices.

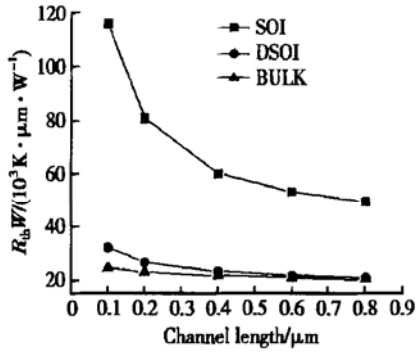

Fig. 6 Normalized thermal resistances from simulation for various device size

5 Conclusion

A novel DSOI MOSFET is fabricated based on local SIMOX technique. This technique is fully compatible with bulk-Si and SOI technique. Both simulation and measurement results prove that such kind of devices have much lower thermal resistance than complete SOI MOSFETs. Self-heating effect is suppressed successfully to the level close to that of bulk devices. This advantage can stay in deep sub-micron realm. DSOI devices can be easily fabricated with SOI devices in the same die, so DSOI can be a promising technique to meet the need of integration of high and low power devices together.

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采用局域注氧技术制备的新型 DSOI 场效应晶体管的热特性*

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摘要: 通过局域注氧工艺, 在同一管芯上制作了 DSOI、体硅和 SOI 三种结构的器件. 通过测量和模拟比较了这三种结构器件的热特性. 模拟和测量的结果证明 DSOI 器件与 SOI 器件相比, 具有衬底热阻较低的优点, 因而 DSOI 器件在保持 SOI 器件电学特性优势的同时消除了 SOI 器件严重的自热效应. DSOI 器件的衬底热阻和体硅器件非常接近, 并且在进入到深亚微米领域以后能够继续保持这一优势.

关键词: DSOI; SOI; 局域注氧技术; 自热效应; 热阻

EEACC: 2530F; 7320R

中图分类号: TN386　　**文献标识码**: A　　**文章编号**: 0253-4177(2003)02-0117-05

* 国家自然科学基金(批准号: 59995550-1)和国家重点基础研究专项经费(编号: G2000036501)资助项目

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2002-07-23 收到, 2002-10-09 定稿