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Simulation of a Silicon LED in Standard CMOS Technology*

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Abstract: A reverse bias silicon p-n junction based on light emitting diode is designed in standard 0.6μm industrial CMOS technology. The mechanism of the light emitting of this device is discussed. The device is simulated by the commercial software. *I-V* characteristic under forward or reverse bias is simulated utilizing the commercial software. The results between simulation and experiment data are compared. The results show that it is a promising device and may find applications in light linking.

Key words: reverse bias silicon p-n junction; silicon based LED; breakdown voltage; CMOS
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1 Introduction

There has been a renewed attempts to realize a silicon LED in standard industrial CMOS technology in the past over 10 years for being fully integrated with the silicon integrated circuits(IC). That reverse bias silicon p-n junction can emit visible light operating in the avalanche mode was first reported in 1955[1]. From this origin work some emission mechanisms[2~5] were established and some devices were fabricated in standard CMOS technology[4~8]. The external quantum efficiency (EQE) of these devices is $\sim 10^{-5}$ and not comparable to the Ⅲ-Ⅴ compounds light sources, but the advantage of silicon based LED is that they can be cheaply and easily integrated with silicon IC. The measured optical power is about four orders of magnitude higher than the detectability limit of Si detectors of corresponding area. These kinds of LEDs may find applications in next generation IC.

In this paper, a silicon based LED was designed in a standard industrial 0.6μm CMOS technology. The emission mechanism of this device was discussed and a proper physical model was established. According to the physical model some design suggestions were made to increase the EQE and optical power. The *I-V* characteristics under forward and reverse bias were simulated by commercial software. The influence of the doping concentration of the p well was also discussed by simulation. To modulate the light intensity a poly-gate was designed on top of the active region and the modulation results was also simulated.

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2 Emission mechanism discussion

Some mechanisms have been proposed to explain the origin of the visible emission from reverse bias p-n junctions such as first a Bremss-trahlung[2] model and a intra-conduction-band transition model[3], later a interband electron and hole recombination model[4]. All these models can accord with their experiments very well, but can not explain all the luminescence phenomena from silicon reverse bias p-n junctions. Under this condition, Akil *et al.*[5] gave a multi-mechanism model (illustrated in Fig. 1) for avalanche emission from reverse bias silicon p-n junctions. According to their analysis photons with different energies are emitted by different mechanism. Below ~ 1.8eV is indirect interband emission, above ~ 2.3eV is direct interband emission and the intermediate is intraband Bremss-trahlung emission.

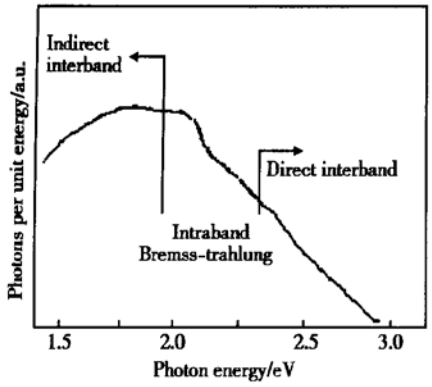

Fig. 1 Emission mechanism of reverse biased silicon p-n junction

According to Akil's multi-mechanism model the optical intensity had a linear relationship vs diode current and this prediction was tested by all the experiments data in the past[4,6~8]. This can be explained by the following: in avalanche breakdown mode, emission is essentially caused by the carriers accelerated by the high electrical field. The hot carriers can create electron-hole pairs through charge multiplication process. The light intensity is equal to that of the photons emitted by electron-hole recombination and this depends on $n+p$, where n, p are the numbers of minority electrons and holes injected into the depletion region. That leads to the linear relationship.

3 Device design

According to the emission mechanism analysis, our approach to realize a silicon based light emitting device relies on the following:

(1) utilizing a reverse bias shallow silicon p-n junction for light emission;

(2) utilizing a standard industrial 0.6μm CMOS technology;

(3) confining the p-n junction close to the surface to minish the optical absorption loss;

(4) utilizing a poly-Si on top of the depletion region for modulating the light intensity.

Figure 2 shows the schematic of the device. The device is designed utilizing a 0.6μm p well standard CMOS technology. The n^+ ($5\times10^{20}cm^{-3}$) region and p($5\times10^{18}cm^{-3}$) region is embedded into a p^- type substrate with a doping concentration of $1\times10^{15}cm^{-3}$ and the junction depth is 0.4μm. This n^+-p junction is made close to the surface to minish the absorption loss and may contribute to light emission for size effect. The poly-Si layer is on top of the p region because the depletion region always mainly extends to the lightly doping region. The light is expected to be emitted from the depletion region. Because the light emission would occur only if the p-n junction is reverse biased, the Ohmic contact on top of n^+ region is taken as a source(see Fig. 2).

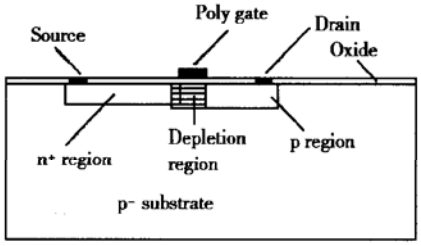

Fig. 2 Schematic of the device structure

4 Simulation results

4.1 Forward bias *I-V* characteristics

Figure 3 shows the forward *I-V* characteristics of the simulation results. The source bias augments from 0 to 18V and correspondingly the junction current from 0 to 0.8A. There is no remarkable difference comparing to the traditional *I-V* curves of silicon p-n junctions. This result indicates that the device can work normally under forward bias conditions.

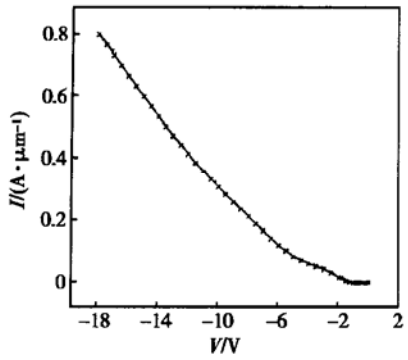

Fig. 3　Forward *I-V* characteristics of silicon p-n junction

4.2 Reverse bias *I-V* characteristics

Figure 4 shows the reverse bias *I-V* characteristics of the simulation results. The breakdown voltage is more than 6V and this ensures the main breakdown

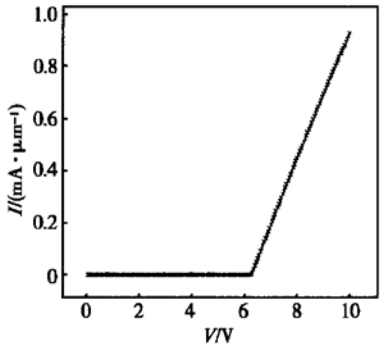

Fig. 4　Reverse bias *I-V* characteristics

mode is avalanche. There is a linear dependence of current vs source bias after breakdown. According to the above analysis there is a linear dependence of optical intensity vs reverse current so that it will also be a linear dependence of optical intensity vs source bias.

4.3 Influence of p region doping concentration on breakdown voltage

Figure 5 shows the relationship between p region doping concentration and breakdown voltage. With the doping concentration increasing from 10^{16} to 5×10^{18} cm^{-3}, the breakdown voltage decreases from 20.3V to 5.0V. The breakdown voltage is above 5.0V and this ensures the main breakdown mode is avalanche. The simulation result can be explained by

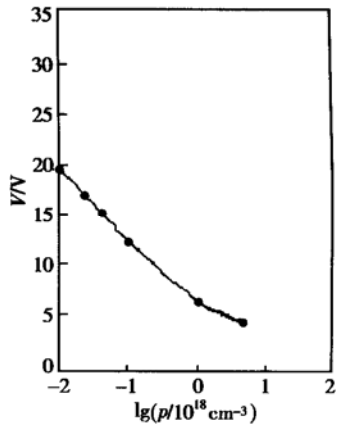

Fig. 5　Influence of p region doping concentration on breakdown voltage

the following: If the junction is reverse biased, the minority carriers are injected into the depletion region and accelerated by high electrical field. If the hot carriers can be accelerated enough, charge multiplication processes can be created. These processes will cause junction breakdown and consequently the breakdown is correlated with the numbers of the injected minority carriers. Higher p region doping concentration will add the holes injected into the depletion region and consequently lower the breakdown voltage. Similar results were reported by Plessis[9]: the n^+ to p well diodes exhibited avalanche breakdown at 18.5V, and the n^+ to p^+ diodes had a field emission breakdown voltage of 4V. To be a practical device the working voltage must be lower than 5V. Some special structures of the device for lowering the working voltage were proposed by Snyman[10] and Matjila[11]. These results show that this device can be a low voltage

LED.

4.4 Influence of gate bias on light intensity

Light intensity modulation results of gate bias are simulated. Figure 6 shows varying the gate bias results in the modulation of junction current and light intensity and the source bias is kept constantly at a value of 8V. A near quadratic relationship of junction

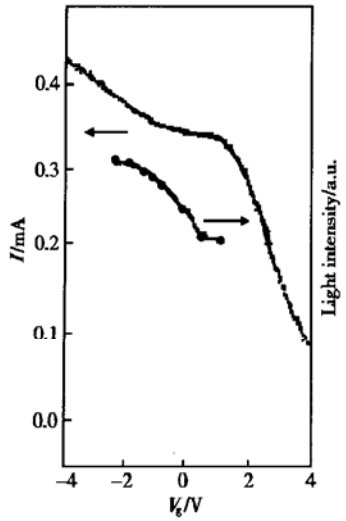

Fig. 6 Modulation effect of gate bias at constant anode bias

current and gate bias, consequently the near quadratic relationship between junction current and light intensity are all illustrated. If the negative gate bias is applied, the holes will accumulate near the surface of the p region underneath the poly-Si layer. This accumulation will enhance the holes density and at the same time strengthen the electrical field there. The result is that the light emission is strengthened, which means larger negative gate bias results in larger light emission intensity. If a positive gate bias is applied, there will be the accumulation of electrons in the p region underneath the poly-Si layer. During this process recombination between electrons and holes minishes the carriers density in p region. Accordingly the junction current is minished at constant source bias. So that the light intensity is also minished. From this analysis, larger positive gate bias causes less light emission. Plessi's[7] calculation showed that the junction current and light intensity is proportional to $-V_g^2$(gate bias). This simulation result gives a nice accord with Pless's experiment data.

5 Conclusion

In this paper a silicon based light emitting device is designed in standard industrial CMOS technology and simulated by commercial software. Theoretical analysis shows that the optical intensity is proportional to junction current and this device can be a low voltage device (below 5V). The light intensity can be modulated utilizing a poly-Si gate. Some of other characteristics such as long term reliabilities, optical power, etc. should be tested by experiment determinations. For it can be realized in standard CMOS technology, this Si LED will be a promising device.

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与标准 CMOS 完全兼容的硅基 LED 器件模拟*

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摘要：采用工业标准 0.6μm CMOS 工艺设计了以反向击穿硅 p-n 结为基础的光发射器件. 讨论了该器件的光发射机理. 利用商业模拟软件对器件的工作特性进行了模拟，包括器件的正向和反向 *I-V* 特性、p 区掺杂浓度对击穿电压的影响以及门电压对器件发光强度的调制特性的影响等. 结果表明该器件是一种很有前途的硅发光器件，在光互连等领域具有广阔的应用前景.

关键词：反向击穿硅 p-n 结；硅基光发射器件；击穿电压；CMOS

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