# Analysis and Design of an Accelerometer Fabricated with Porous Silicon as Sacrificial Layer\*

Zhou Jun<sup>1</sup>, Wang Xiaohong<sup>1</sup>, Yao Pengjun<sup>2</sup>, Dong Liang<sup>1</sup> and Liu Litian<sup>1</sup>

(1 Institute of Microelectronics, Tsinghua University, Beijing 100084, China)
(2 School of Information Technology, Shenyang Normal University, Shenyang 110036, China)

Abstract: A piezoresistive silicon accelerometer fabricated by a selective, self-stopping porous silicon (PS) etching method using an epitaxial layer for movable microstructures is described and analyzed. The technique is capable of constructing a microstructure precisely. PS is used as a sacrificial layer, and releasing holes are etched in the film. TMAH solution with additional Si powder and (NH<sub>4</sub>) 2S<sub>2</sub>O<sub>8</sub> is used to remove PS through the small releasing holes without eroding uncovered Al. The designed fabrication process is full compatible with standard CMOS process.

Key words: accelerometer; porous silicon; micromachining; sacrificial layer; MEMS

EEACC: 0580; 7280; 2575; 8460

CLC number: T N 304 Document code: A Article ID: 0253-4177(2003) 07-0687-06

### 1 Introduction

Relevant researches of micro-electromechnical systems have emerged in recent years as a result of the urge of product of miniaturization. Microsensors are essential to the integration of electric and mechanical systems and consist of microstructures, displacement transducers, and signal amplifiers, which can be easily integrated into a single chip by using the existing manufacturing processes, such as bulk— and surface—micromachining techniques. However, in bulk—micromachining, besides the following drawbacks (for instance, the mask pattern on the backside of a wafer should be larger than desired frontside pattern, this limits the maximum packaging density), the main problem is that the

technique is not compatible with the standard CMOS process, so it is difficult to get MEMS and IC integrated. All these drawbacks can be overcomed by using surface-micromachining technology. In this technology, a sacrificial layer is deposited, and the maximum distance from the microstructure to the substrate is given by the thickness of the sacrificial layer. It is limited to a few micrometers<sup>[1]</sup>. The usual polycrystalline silicon widely used in surface-micromachining has poor mechanical properties compared to those of single-crystalline silicon.

Using PS as a sacrificial layer can overcome all the above-mentioned drawbacks. PS is produced by electrochemical dissolution of silicon in HF. Its formation rate depends on the concentration of HF and the current density, as well as the impurity and

<sup>\*</sup> Project supported by National Basic Research '973" Foundation of China (No. G1999033108), and Tsinghua University Basic Research '985" Foundation (No. 199925001)

Zhou Jun male, was born in 1978, graduate student. He is engaged in the research on the integration and process of semiconductor sensors.

Wang Xiaohong female, was born in 1963, associate professor and postdoctor. She is engaged in the research on semiconductor devices and MEMS.

concentration of the substrate<sup>[2]</sup>. Generally speaking, the order of its formation rate is: n<sup>+</sup> > p<sup>+</sup> > p> n<sup>[3]</sup>. So highly-doped areas can be locally defined on the Si substrate by diffusing or ion implanting. PS may be first generated in the highly-doped regions quickly, which expresses the selectivity of PS formation. In this technique, single-crystalline epitaxial silicon can be used as a structural layer, and the sacrificial layer may be removed in TMAH or weak KOH at room temperature instead of aggressive HF.

In this paper, a piezoresistive silicon accelerometer based on PS etching method is analyzed and discussed.

# 2 Structure design

There have been many structures for piezoresitive accelerometers. They are common beam-mass structures, such as single beam, double beams, four beams, twin-mass five beams structure<sup>[4-6]</sup>, etc.

In piezoreisistive accelerometers, the piezoresistive element is formed in the supporting beams. The device sensitivity is defined as the relative change of resistance per unit of acceleration g.

$$s = \frac{\Delta R}{Rg} \tag{1}$$

where  $\Delta R/R = K\epsilon$ . The factor K depends on the orientation of piezoresistors relative to the crystal and its doping level, and the strain  $\epsilon$  is linear function of the stress. In most cases of MEMS, the main contribution is the normal direction. Therefore, the normal stress  $\epsilon$  in the place of piezoresisors can be approximated by  $\sigma_m$ ,

$$\epsilon = \frac{\sigma_{\rm m}}{E} \tag{2}$$

where E is the Young's modulus of the material. Combining Eqs. (1) and (2), and introducing  $K_P = K/E$ , the physical sensitivity of the device is

$$s = K_{\rm P}\sigma_{\rm m}$$

which means that the device sensitivity of an accelerometer is proportional to the normal stress in the place of the piezoresistive element. Therefore, the analysis of the stress distribution is necessary and finite-element analysis (FEA) has shown that the maximum normal stress due to bending is concentrated at the root of supporting beams.

Figure 1 shows five basic suspension configurations of accelerometer mechanical structures, and all the supporting beams and seismic masses are of the same size separately. In order to calculate the stress theoretically at the root of the beams, we ob-

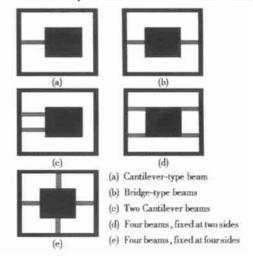


Fig. 1 Schematic diagram of mechanical structures

tain the simplest "beam and mass" model: the weight of the supporting beams is negligible compared with the seismic mass that can be considered as a particle, the deflection of supporting beams observe linear elasticity and Hooke's law. In this case, for instance, the maximum normal stress of the structures of Figs. 1 (a) and (b) due to bending is:

$$\sigma_{\text{m}} = \frac{3ma}{bh^2} (2L_1 + L_2)$$
 (Cantilever-type)  
 $\sigma_{\text{m}} = \frac{3ma}{bh^2} L_1$  (Bridge-type)

where m and  $L_2$  are the mass and length of seismic masses; b, h, and  $L_1$  are the width, thickness, and length of supporting beams separately; a is the acceleration. It is obvious that because the cantilever beam offers the highest degree of freedom and better sensitivity when compared to other structures such as the bridge-type beams, the maximum stress at the root of cantilever-type (single beam struc-

ture) is much larger than that of other structures, which can be also verified by finite-element analysis.

FEA of the structures in Fig. 1 are carried out with Ansys 5. 7, and the results of maximum normal stress are given in Table 1.

Table 1 Results of finite-element analysis of structures

No.	Maximum normal stress/(10 <sup>-6</sup> N • μm <sup>-2</sup> )
(a)	1. 44326
(b)	0. 23625
(c)	0. 90294
(d)	0. 11330
(e)	0. 12024

Table 1 shows that device sensitivity of single-beam and double-beam structures are better than that of four-beam structures, and they are simple in structure design. But their across sensitivities are very large, which can hardly be ignored. On the other hand, the centered seismic mass suspended by four beams will only vibrate along z-axis with negligible motions in other direction.

So, considering the across sensitivity, we adopt the accelerometer configuration of four beam suspensions as shown in Fig. 2. FEA for this structure is carried out in details, and the results are shown in Fig. 3. The stress is concentrated in a very small area at the root of the beams, with little stress in

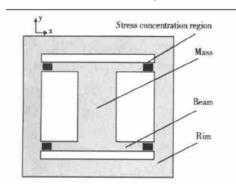


Fig. 2 Schematic diagram of the accelerometer mechanical structure

other regions of the beams. Meanwhile, the stress has good direction. Figure 3 shows that the x directional stress is several times larger than the y directional stress, which explains the main stress is most significant for the mass-beam piezoresistive

effect, other stresses can be ignored. Therefore, different resistors lying in the same beam are affected by the same stress, only when piezoresistive coefficient is different, piezoresistive effect is different.

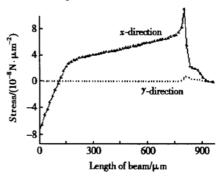


Fig. 3 Stress distributing of an accelerometer beam

# 3 Technique of using PS as a sacrificial layer in MEMS

#### 3. 1 PS preparation and forming selectivity

PS is produced by electrochemical dissolution of silicon in HF, and the electrochemical cell used in fabricating PS is shown Fig. 4. PS is formed in the surface of silicon substrate towards the cathode.

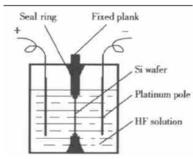


Fig. 4 Electrochemical cell used in fabricating PS

PS forming selectivity is studied in detail. (100)-oriented, 14~ 20Ω·cm, n-type silicon wafers were used as starting materials. A 4μm thick n<sup>+</sup> region, which serves as a sacrificial layer and yields the air gap, was selectively formed by phosphorus implantation followed by an annealing in N<sub>2</sub> atmosphere. LPCVD poly silicon and silicon nitride were deposited respectively and structured. The silicon nitride layer serves as a masking layer

for the protection of poly silicon in PS formation. PS was then formed in the highly-doped regions. Figure 5 can show PS forming selectivity definitely: the lateral size of PS under poly silicon film is approximately  $15\mu$ m and the depth  $4\mu$ m, which is consistent with the outline of the highly-doped areas.

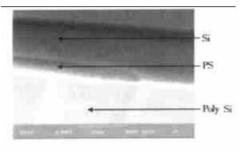


Fig. 5 Cross-sectional SEM view of PS

#### 3. 2 PS sacrificial layer removing

Generally speaking, PS can be removed in every anisotropic silicon etchant, including inorganic aqueous solutions of KOH, NaOH, and NH4OH, as well as organic aqueous solutions, such as TMAH and ethylenediamine pyrocatechol (EDP). To remove PS quickly, 0.5% ~ 1% KOH solution is recommended because of its high etching rate and low cost. However, it is not compatible with the standard CMOS process. So, in order to achieve CMOS compatibility, TMAH solution can be used<sup>[7]</sup>. The use of TMAH solution for etching is gaining popularity for its relative non-toxicity compared to EDP and its CMOS compatibility because it has no K+ ion. At the same time, dissolving some silicon particles in TMAH can decrease the aluminum etching rate. Researchers have reported a silicon etchant with zero aluminum etching rate. This etchant consists of 5wt. % TMAH solution, 1.4wt. % (or above) dissolve silicon, and 0.4wt.%~ 0.7wt.% (NH4)2S2O8 oxidant additive[8]. In this way, a full CMOS compatible process of sacrificial layer etching can be achieved.

In order to obtain a wide-dimensional freestanding microstructure film, regularly ranged releasing holes may be made in the microstructure film to provide flowing access of the anodization current. More important, PS under the film will be etched via the releasing holes. The distributing of releasing holes has to be considered seriously to assure the efficiency of PS removing, as well as the reliability of the structure. After TMAH etching via releasing holes, a freestanding structure will be achieved.

# 4 Fabrication and test

A highly selective PS surface-micromachining technique without any undercutting problem in fabricating piezoresistive accelerometer with four beams is developed. Based on the experiment on PS fabrication and removing, we designed a new method to fabricate the single-sided Si accelerometer. The designed sequence for the fabrication is shown in Fig. 6. It starts with (100) -oriented, 10~ 20Ω • cm, n-type silicon wafers.

A  $10\mu m$  thick  $n^+$  region, which serves as a sacrificial layer and yields the air gap, is selectively formed by phosphorus implantation. The doping density of the  $n^+$ -buried layer must be higher than  $1\times 10^{17} {\rm cm}^{-3}$ , high enough to be anodized in HF solution. The backside of the wafer is also heavily implanted with phosphorus to provide a uniform current density during anodization (Fig. 6(a)).

A low-doped n-type epitaxial layer, which is used for movable microstructures, is deposited on the substrate. The piezoresistors are formed by boron ion implantation and followed by annealing at  $1150^{\circ}$ C in N<sub>2</sub> atmosphere. The desired junction depth and sheet resistance of the piezoresistors are about  $1\mu m$  and  $200\Omega/\Box$ , respectively (Fig. 6(b)).

A 20nm thick silicon dioxide is thermally grown on the substrate as a low-stress layer. 80nm thick LPCVD Si<sub>3</sub>N<sub>4</sub>, 150nm poly silicon, and then 120nm Si<sub>3</sub>N<sub>4</sub> are deposited respectively, which serve as a masking layer for PS formation (Fig. 6(c)).

The masking layer is patterned by plasma and wet chemical etching, and the uncovered part of nepitaxial silicon layer is removed by ICP. Some holes are made in the microstructure film to provide flowing access of the anodization current and also serve as releasing holes for PS (Fig. 6(d)).

PS is formed by etching in 10% aqueous HF solution at room temperature with a constant current density of  $20 \text{mA/cm}^2(\text{Fig. 6(e)})$ .

LPCVD LTO 500nm, and then  $1\mu m$  thick aluminum is spattered and etched (Fig. 6(f)).

5% TMAH solution (also consists of 1.6% dissolved silicon and 0.6% (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub>) is used to remove PS via releasing holes, and the small Si is attached on the film to improve the weight of the mass. (Fig. 6(g)).

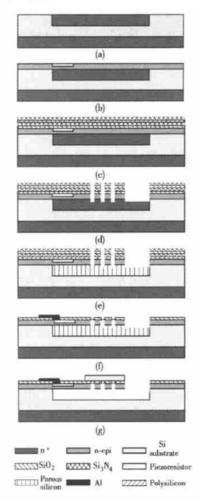


Fig. 6 Fabrication process of the accelerometer

Therefore, the completed accelerometer consists of a loaded mass at the centre of the structure, four beams supporting a mass. The accelerometer detects excited motion with a full-

bridge circuit, composed of four piezoresistor arms on the cantilever beams. Figure 7 shows the linear characteristic of the device in the acceleration range  $0\sim 10 \mathrm{g}$ . The output deviation of each bridge was about  $\pm 3\%$ , possibly due to misalignment between the center of the mass and the center of the mass paddle and variations in piezoresistors. As shown in Fig. 7, a linearity test for the microfabricated accelerometer results in a sensitivity of  $100\mu V/g$  at a resistor bridge input voltage of 3V, and  $350\mu V/g$  at the input voltage of 5V.

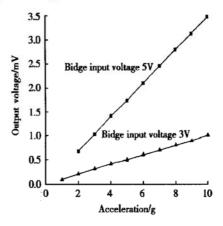


Fig. 7 Linearity of the accelerometer response for the acceleration range 0~ 10g

# 5 Conclusion

This paper presents the fabrication of an accelerometer, and PS is used as a sacrificial layer.

The designed mechanical structure with four beams not only can decrease cross-axis sensitivity, but also utilize full strain caused by the acceleration. Using finite-element analysis software, we did strain simulation to analyze the stress distribution, and the result agrees with theory analysis very well.

PS is used as a sacrificial layer. The highly selective, self-stopping PS surface-micromachining technique on a selectively implanted (100)-oriented n/n<sup>+</sup>/n substrate without experiencing any lateral etching or undercutting problem makes it possible to define precisely the dimensions of the beam and the air gap of the microstructure by controlling the

thickness of the n-epitaxial and n<sup>+</sup> regions. At the same time, TMAH solution with additional Si pow-der and (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub> can be used to remove the PS layer through small releasing holes without eroding the uncovered Al. The fabrication process is full compatible with CMOS process. Then, a good accelerometer is designed and fabricated.

#### References

- [1] Bustillo J M, Howe R T, Muller R S. Surface micromachining for microelectromechanical systems. Proc IEEE, 1998, 86: 1552
- [2] Beale M I J, Benjamin J D, Uren M J, et al. An experimental and theoretical study of the formation and microstructure of porous silicon. J Cryst Growth, 1985, 73: 622
- [3] Lang W, Steiner P, Sandmaier H. Porous silicon: a novel ma-

- terial for microsystems. Sensors and Actuators, 1995, A51: 31
- [4] Roylance L M, Angell J B. A batch-fabricated silicon accelerometer. IEEE Trans Electron Devices, 1979, ED-26: 1911
- [5] Takao H, Matsumoto Y, Ishida M. A monolithically integrated three-axis accelerometer using CMOS compatible stresssensitive differential amplifiers. IEEE Trans Electron Devices, 1999, ED-26: 109J
- [6] Zhu Haijun, Chen Hong, Bao Minhang. Design and characterization of silicon lateral accelerometer. Chinese Journal of Semiconductors, 1997, 18(7):518(in Chinese)[朱海军, 陈宏, 鲍敏杭. 横向加速度传感器设计及特性研究. 半导体学报, 1997, 18(7):518]
- [7] Thong J T L, Choi W K, et al. TMAH etching of silicon and the interaction of etching parameters. Sensors and Actuators, 1997, A63: 243
- [8] Yan Guizhen, Chan Philip C H, et al. An improved TMAH Sietching solution without attacking exposed aluminum. Proceedings of the IEEE Micro Electro Mechanical Systems (MEMS), 2000: 562

# 基于多孔硅牺牲层技术的压阻式加速度传感器的分析和设计\*

周 俊 王晓红 姚朋军 董 良 刘理天

(1清华大学微电子学研究所, 北京 100084)

(2 沈阳师范大学信息技术学院, 沈阳 110036)

摘要:分析并设计了一种利用高选择自停止的多孔硅牺牲层技术制作压阻式加速度传感器的工艺,并利用外延单晶硅作为传感器的结构材料,这种工艺能精确地控制微结构的尺寸.利用多孔硅作牺牲层工艺,使用加入硅粉和 (NH4) 2S2O8 的 TMAH 溶液通过在薄膜上制作的小孔释放多孔硅,能很好地保护未被覆盖的铝线.该工艺和标准的 CMOS 工艺完全兼容.

关键词: 加速度传感器; 多孔硅; 微加工; 牺牲层; 微机电系统

EEACC: 0580; 7280; 2575; 8460

中图分类号: TN 304 文献标识码: A 文章编号: 0253-4177(2003)07-0687-06

<sup>\*</sup> 国家重点基础研究发展规划(No. G1999033108)及清华大学 985 基础研究基金(No. 199925001)资助项目

周 俊 男,1978年出生,研究生,研究方向为半导体传感器的集成和工艺.