Polysilicon Emitter Double Mesa Microwave Power SiGe HBT[*]

Liu Zhinong, Xiong Xiaoyi, Huang Wentao, Li Gaoqing, Zhang Wei, Xu Jun, Liu Zhihong,

Lin Huiwang, Xu Ping, Chen Peiyi and Tsien Pei-Hsin

(*Institute of Microelectronics, Tsinghua University, Beijing 100084, China*)

Abstract: A new 125mm UHV/CVD SiGe/Si epitaxy equipment SGE500 capable of commercialization is constructed and device-level SiGe HBT material is grown. A polysilicon emitter (PolyE) double mesa microwave power SiGe HBT showing excellent low current DC characteristics with $\beta = 60@\ V_{CE}/I_C = 9.0V/300\mu A$, $\beta = 100@\ 5V/50mA$, $BV_{CBO} = 22V$, $f_t/f_{max} = 5.4GHz/7.7GHz@\ 3V/10mA$ is demonstrated. The PolyE SiGe HBT needs only 6 lithographical steps and cancels the growth of the thick emitter epitaxy layer, both of which show great potential for volume production. A 60-finger class-A SiGe linear power amplifier (PA) with 22dBm of 1dB compress point output power (P_{1dB}), 11dB of power gain (G_p) and 26.1% of power added efficiency (PAE) @ 900MHz, 3.5V/0.2A is demonstrated. Another 120-finger class-A SiGe PA with 33.3dBm (2.1W) of P_{out}, 10.3dB of G_p and 33.9% of PAE @ 900MHz, 11V/0.52A is also demonstrated.

Key words: SiGe; HBT; microwave power amplifer

EEACC: 2520M; 2560J; 1350F

CLC number: TN323$^+$.4   **Document code:** A   **Article ID:** 0253-4177(2003)09-0897-06

1 Introduction

The high-performance, high-integration, high-volume, and high-efficient SiGe IC could produce small factor form, long battery life, fast information and data transmission rate and high communication quality of service. Since SiGe was introduced into the industry in 1998, it has fleetly involved into mainstream and created one of the most successful semiconductor miracles in such a short period of less than five years. SiGe explosively increased its market share in almost all the RF communication fields like 2G/3G mobile communication, 2.4GHz Bluetooth, 2.4 ~ 5.0GHz IEEE802.11a/b/g, up to 40Gbps optical communication, GPS, TV tuners, high-speed ADC and even ultra-fast 5GHz FPGA[1].

The revised Johnson limitation says $BV_{CEO} \times f_t$ approximately equals 300GHz·V, which is a basic obstacle for RF power amplifier (PA), especially for high-breakdown case. SiGe technology now begins to challenge the role of GaAs and LDMOS in mobile communication base station PA. Recently Johansson et al.[2] reported a 25V/20W SiGe power transistor under 2GHz AB class CW condition for Cellular base station.

2 SGE500 and device structure

The soul of SiGe HBT is the strained Si/SiGe/Si multi-layer structure, the crystal quality, and material parameters of which are directly determined by the

epitaxy equipment. A new 125mm single-wafer UHV/CVD SiGe epitaxy equipment SGE500 capable of commercialization is constructed. Compare to its predecessor SGE400[3], SGE500 obtains a considerable improvement. It adds a pre-loaded chamber to further isolate the reactive chamber from the atmosphere environment, and the base vacuum of the reactive room could reach beyond 5×10^{-7} Pa. SGE500 could raise the temperature at a rapid speed of up to 150 ℃/min and the precisely controllable temperature range is broadened to 500~900 ℃. The SiGe layer growth rate is typically 3~8nm/min.

The vertical structure of the PolyE SiGe HBT is shown in Fig. 1. The n^+ (100) silicon substrate is chosen to reduce the bottom collector series resistance. The thickness (W_c) and doping concentration (N_c) of the n^- collector are chosen to satisfy the application-specific demands of BV_{CBO} and maximum collector current density (J_c) and f_t. Key parameters of the base are germanium content x (at present, we just chose the constant x across base zone to simplify

Polysilicon emitter: d=200nm

i-Si emitter: d=20~30nm

SiGe base: x=0.22, N_b=10^{19}cm^{-3}, W_b=50~60 nm

i-SiGe: x=0.22, d=7~10 nm

n-collector: W_c=3μm, N_c=1.5×10^{16}cm^{-3}
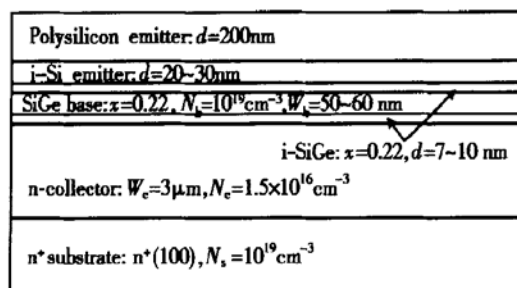
n^+ substrate: n^+(100), N_s=10^{19}cm^{-3}

Fig. 1 Vertical structure of PolyE SiGe HBT

the material growth process), base thickness W_b, and base doping concentration N_b. The main design factors are DC current gain (β), base intrinsic sheet resistance (R_b) and f_t. When W_b dropped, β and f_t would rise while R_b increased, then we could raise N_b to maintain rational R_b. Unlike Si BJT, SiGe HBT could provide additional x to increase β exponentially, and therefore permit thinner W_b and heavier N_b (two orders higher than that of Si BJT) to ensure proper β, optimized f_t and pretty lower R_b, and thus optimized maximum oscillation frequency (f_{max}). The thin i-SiGe layers across both BE and BC junction are

carefully designed to prohibit out-diffuse of boron from base to undoped emitter layer (i-E) and light-doped collector. The i-E layer would form true light-doped emitter layer after total post anneal steps, which could greatly reduce the BE junction capacitance as to improve f_t. On the other hand, it must be thin enough for the poly impurity to diffuse into it and to ensure low emitter resistance. Present design selects a thickness of about 20~30nm. The top 200nm thick polysilicon layer is deposited using LPCVD, which will be discussed in the next section. Please Refer to Refs. [3, 4] for the detailed SiGe HBT material growth process.

The lateral structure is a little different from the one discussed in Ref. [5]. The emitter mesa is 1.6μm wide, the distance between the emitter mesa and B-hole is 1.2μm, and the B-hole and E-hole are both 0.8μm wide. The emitter stripe is 40μm long which is chosen to provide higher current and power output capabilities.

L_E=40μm

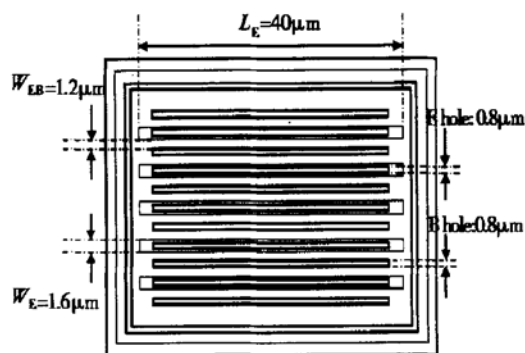W_{EB}=1.2μm

B-hole: 0.8μm

B-hole: 0.8μm

W_E=1.6μm

Fig. 2 Lateral structure of PolyE SiGe HBT

3 PolyE double mesa SiGe HBT process

The process is somewhat like the one reported in Ref. [5], the main improvement would be:

(1) PolyE process. 200nm thick polysilicon (poly) is carefully deposited using LPCVD at 625 ℃, which is then implanted with phosphorous at a dose of 5×10^{15}cm^{-2} and energy of 70keV. The clean step before poly deposition, the ion implantation and post anneal thermal budget have to be carefully designed to

satisfy the multiple demands of the transistor, which would be further reviewed in list (4).

(2) Sidewall process. Lateral size of the sidewall is a key step to the trade-off between R_b and BE junction leakage current. A 300nm LPCVD SiO_2 is deposited and then anisotropical RIE is used to maintain a lateral size of about 150~ 200nm.

(3) Hole dielectric and hole-drilling process. 150nm LPCVD SiO_2 and 200nm PECVD Si_3N_4 are deposited as the hole dielectric. When the hole dielectrics is RIE etched to about 10~ 20nm, 1：100 buffered HF solution is used to wet-etch the remain thin layer to acquire clean and damage-free hole. The compound hole dielectric and the two-step hole-drilling process greatly improve the low current performance and cut down the collector leakage current.

(4) Total thermal budget. The total low thermal budget required by SiGe material puts a stringent demand on the post annealing condition. The doping impurity in the poly has to be activated effectively and some part of it ought to diffuse into i-E layer to form a light-doped emitter. Extrinsic base and emitter contact resistance need to be lowered rationally. Out-diffuse of boron in the base to the collector and i-E layer and relief of the strained SiGe base zone under somewhat high temperature have to be simultaneously considered carefully. A two-step solution is adopted to tackle all of the upper aspects. Low temperature furnace annealing is first made to activate the doping, reduce possible crystal defect, diffuse the doping impurity from poly to the i-E layer, then RTA further reduce the contact resistance and activate the doping.

(5) Metal process. 1μm thick Al is sputtered at a substrate temperature of about 250 ℃ to permit the stable and good contact formation. The alloy condition is 430 ℃/30min, which is chosen according to the trade-off between contact resistance and collector current leakage based on a great deal of temperature change experiments.

(6) Compatible with the standard Si CMOS technology. It is meaningful to note that the whole PolyE SiGe HBT process is super simple with only 6 lithographical steps and compatible with the current CMOS process and now under the small volume production development. Figure 3 gives the final device structure.
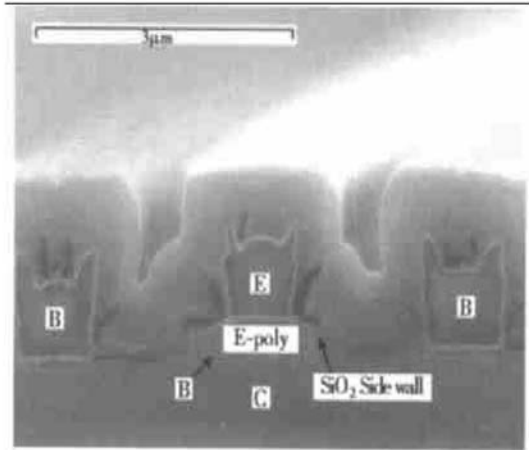

Fig. 3　Final HBT device structure

4　DC characteristics

The transistor's DC characteristic is measured using Keithley 4200. Figure 4 shows the reverse breakdown characteristic of EB and CB junctions. The BC junction breakdown voltage is about 22V, which is very hard and the leakage is pretty low (91nA@ 20V, 10-finger transistor). The BE junction breakdown voltage is about 3V and somewhat soft (3μA @ − 2V), which may be caused by the poly BE junction (i-E layer is very thin for the space-charge-zone to easily extend across the poly layer).

Figure 5 shows the excellent low current DC characteristic: β= 60@ V_{CE}/I_C= 5V/300μA. When collector current increased, β increased also, to about β= 100@ 5V/50mA.

Besides exponentially increased with x in the SiGe base, the introduction of the wider-bandgap PolyE could also further increase β, e. g., a PolyE SiGe HBT with current gain beyond 800@ 5V/50mA is fabricated. The using of PolyE permits a smaller x to provide higher thermal budget or heavier boron concentration to produce lower base resistance, which provides additional flexibility to trade between DC and RF performance.
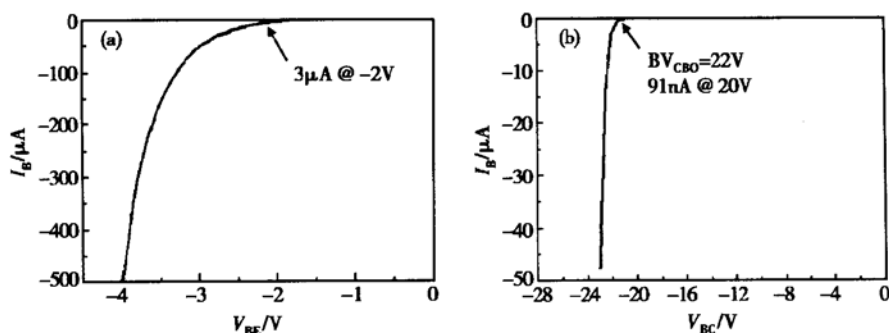
Fig. 4   Reverse breakdown characteristics of BE junction (a) and BC junction (b) BV_{EBO} = 3V, BV_{CBO}= 22V
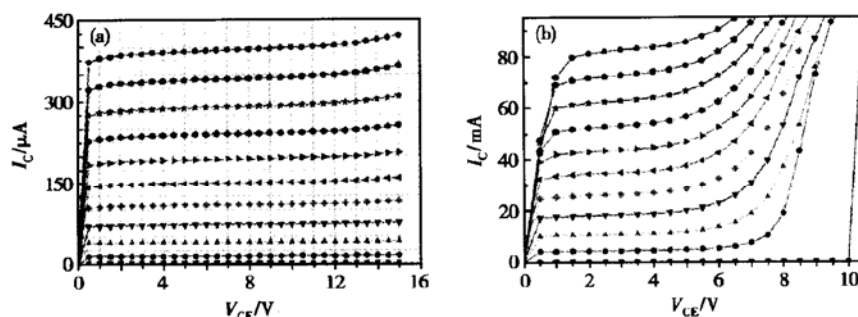

Fig. 5   Output curves with β= 60@ 5V/ 300μA(a) and β= 100@ 5V/ 50mA(b)

After being packaged in a metal ceramic form, scatter-parameter of a 10-finger transistor (emitter area: $10 \times (1.6^{\mu}m \times 40^{\mu}m))$ is measured using HP8510A, from which f_t and f_{max} is deduced (see Fig. 6). The initial result is somewhat lower than expected: f_t/ f_{max}= 5. 5GHz/ 7. 7GHz @ 3V/ 10mA, the detailed reason is under investigation.

Class-A linear PAs using 60-finger and 120-finger PolyE SiGe HBT are made. Figure 7 shows P_{out}, G_p, and PAE curves of the 60-finger-PA at a pretty low DC bias (900MHz, V_{CE}/ I_C= 3. 5V/ 0. 2A). At 1dB compress point, $P_{out}/ G_p/ PAE$= 22dBm/ 11dB/ 26. 1%, as bias increases, the 60-finger SiGe PA gives that of 29. 3dBm (0. 85W)/ 9. 3dB/ 22. 6% @ 9V/ 0. 37A, while the 120-finger SiGe PA gives that of 33. 3dBm(2. 1W)/ 10. 3dB/ 33. 9% @ 11V/ 0. 52A.
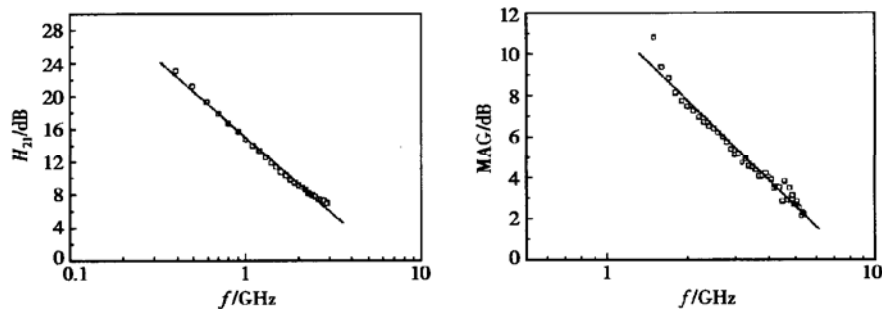

Fig. 6   RF curves of 10-finger PolyE SiGe HBT
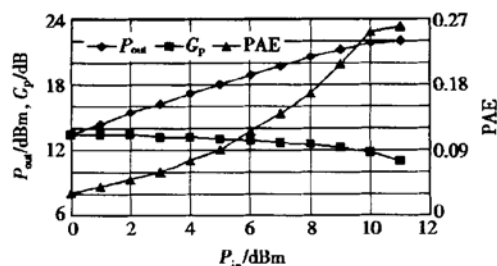
Fig. 7 P_{out}, G_p, PAE versus P_{in} of SiGe PA

5   Conclusion

A new 125mm UHV/CVD SiGe/Si epitaxy equipment SGE500 capable of commercialization is constructed and device-level SiGe HBT material is grown. A PolyE double mesa microwave power SiGe HBT process showing excellent low current DC characteristics with $\beta = 60$ @ 9V/300uA, $\beta = 100$ @ 5V/50mA, $BV_{CBO} = 22V$, $f_t/f_{max} = 5.4GHz/7.7GHz$ @ 10-finger, 3V/10mA is first demonstrated. The poly emitter provides additional flexibility to trade-off between DC and RF performance. The whole process needs only 6 lithographical steps, and is compatible with current CMOS process, and cancels the growth of the thick emitter epitaxy layer, which shows great potential for volume production. A 60-finger class-A SiGe linear PA with 22dBm of P_{1dB}, 11dB of G_p and 26.1% of PAE @ 900MHz, 3.5V/0.2A is demonstrated. Another 120-finger class-A SiGe PA with 33.3dBm (2.1W) of P_{out}, 10.3dB of G_p and 33.9%

of PAE @ 900MHz, 11V/0.52A is also demonstrated.

References

[1]   Liu Zhinong, Tsien Pei-Hsin. Explosively developing SiGe technology. China Integrated Circuit, 2003, to be published(in Chinese)

[2]   Johansson T, Ni Weixin. Feasibility study of 25V SiGe RF-power transistors for cellular base station output amplifiers. Material Science and Engineering B, 2002, 89: 88

[3]   Liu Zhinong, Jia Hongyong, Luo Guangli, et al. Low temperature silicon and silicon germanium doping epitaxy by HV/CVD. Chinese Journal of Semiconductors, 2001, 22(3) : 317(in Chinese) [刘志农, 贾宏勇, 罗广礼, 等. HV/CVD 系统 Si 、SiGe 低温掺杂外延. 半导体学报, 2001, 22(3) : 317]

[4]   Jia Hongyong, Lin Huiwang, Chen Peiyi, et al. Epitaxy of SiGe HBT structure by high vacuum/rapid thermal processing/chemical vapor deposition. Chinese Journal of Semiconductors, 2001, 22(3) : 251

[5]   Jia Hongyong, Zhu Wenbin, Liu Zhinong, et al. Development of microwave SiGe HBT. Chinese Journal of Semiconductors, 2000, 21(10) : 970

多晶发射极双台面微波功率 SiGe HBT[*]

刘志农 熊小义 黄文韬 李高庆 张 伟 许 军 刘志弘

林惠旺 许 平 陈培毅 钱佩信

(清华大学微电子学研究所, 北京 100084)

摘要: 研制成功了可商业化的 75mm 单片超高真空化学气相淀积锗硅外延设备 SGE500, 并生长了器件级 SiGe HBT 材料. 研制了具有优良小电流特性的多晶发射极双台面微波功率 SiGe HBT 器件, 其性能为: $\beta = 60@\ V_{CE}/I_C = 9V/300\mu A$, $\beta = 100@\ 5V/50mA$, $BV_{CBO} = 22V$, $f_t/f_{max} = 5.4GHz/7.7GHz@\ 10$ 指, $3V/10mA$. 多晶发射极可进一步提供直流和射频性能的折衷, 该工艺总共只有 6 步光刻, 与 CMOS 工艺兼容且 (因多晶发射极) 无需发射极外延层的生长, 这些优点使其适合于商业化生产. 利用 60 指和 120 指的 SiGe HBT 制作了微波锗硅功率放大器. 60 指功放在 900MHz 和 3.5V/0.2A 偏置时在 1dB 压缩点给出 $P_{1dB}/G_p/PAE = 22dBm/11dB/26.1\%$. 120 指功放 900MHz 工作时给出了 $P_{out}/G_p/PAE = 33.3dBm\ (2.1W)/10.3dB/33.9\%@\ 11V/0.52A$.

关键词: 锗硅; 异质结双极晶体管; 微波功率放大器

EEACC: 2520M; 2560J; 1350F

中图分类号: TN323[+].4   **文献标识码:** A   **文章编号:** 0253-4177(2003)09-0897-06