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Efficient Interconnect Network Model for Linear Circuit Reduction*

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Abstract: A new interconnect network model for linear network reduction is presented. In this new model, the ports of the interconnect network are classified into two groups: active and passive ports. After the classification, some proprieties of the interconnect network are found to be redundant and pruned before reduction. For common interconnect networks, the scale of reduced models is smaller than 50% of the scale of previous works.

Key words: moment matching; MPVL process; linear circuit reduction
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1 Introduction

As process technology scales to the deep sub-micrometer regime, interconnect plays a more and more important role in current CMOS VLSI. Interconnect RC(L) effect has greater impact than the gate on signal propagation[1]. With the interconnect space reduced and wire aspect ratio increased, another important effect called crosstalk becomes more and more obvious. Commonly, an interconnect network model extracted by CAD tools contains a large number of coupled R-L-C components. Since these extracted circuits are often beyond the capability of simulation tools both in circuit scale and time consuming, reduced-order interconnect models are imperative.

Asymptotic waveform evaluation(AWE)[2] is the first successful circuit reduction tool. But the numerical unstability of this algorithm greatly limited its applications in practical interconnect network reduction. A variety of modified methods[3~6] based on this basic idea have been developed in recent years. The Krylov-subspace based methods, PVL[5] and Arnoldi[6] algorithm, seemed to be very successful in practical network reduction. The multi-input multi-output (MIMO) versions of these algorithms such as MPVL[7], syMPVL[8], block Arnoldi[9], and PRIMA[10] have been integrated into spice-like tools in previous works.

As the scale of VLSI and interconnect density keeps growing, an interconnect network will consist of tens or even hundreds of coupled interconnects. And with the working frequency growing higher, more moments need to be matched in the interconnect reduction. We have observed that the scale of reduced-order circuit grows rapidly with the number of net-

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work ports and matching moments. This trend will have an impact on the reduction efficiency with the development of VLSI.

In this paper, a new interconnect network model for reduction is proposed to abate this impact. According to the properties of the CMOS circuits, parts of the interconnect network's properties are pruned in this new interconnect model before reduction. The results of reduction show that this model greatly improves the efficiency comparing with the previous work, especially with those tree-like networks.

2 Model definition

Figure 1 shows the process of an n-port interconnect network reduction[10]. A much smaller network with analogical external property replaces the original network in the new system. For such a multi-input multi-output time-invariant network, its external properties can be described by Z-parameter as follows:

$$H(s) = B^{\mathrm{T}}(\boldsymbol{G} + s\boldsymbol{C})^{-1}B \qquad (1)$$

here, $\boldsymbol{G}$ and $\boldsymbol{C}$ are the conductance and susceptance matrices. By matching the first q moments, we get a new Z-parameter:

$$\hat{H}_q(s) = H(s) + O(s^q) \qquad (2)$$

The value of q is determined by the demand of accuracy and the complexity of the original network. For RC networks, the reduction result of $q = 2$ is accurate. But for the complexity RCL networks, more moments need to be matched.

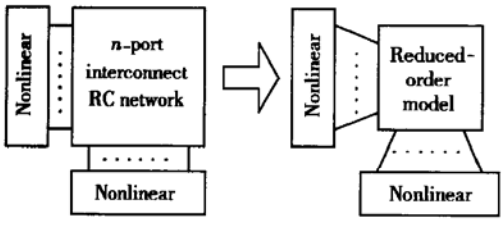

Fig. 1　Interconnect network reduction

In CMOS circuits, we can classify the ports of an interconnect network into two groups as follows:

Passive ports= {port that only connects to the gates of the MOS transistors}

Active ports= {others}

Since the signals on the ports only connected to the gates of MOS transistors will not change actively, we call them "passive" ports. We call all the other ports as "active" ports despite of the fact that signals on some of them will also not change actively. Passive ports and active ports can be easily separated by this definition.

Because the gate capacitance of a MOS transistor is commonly much smaller than that of interconnect, and varies only a little with the input voltage, we can then simply assign them to constant values and absorb them into the interconnect network. Thus, in the newly constructed network, the passive ports are all open ended. Figure 2 shows such a preprocess of an n-port network(p active ports and m passive ports, $n = p + m$). Here, $\boldsymbol{C}_{\mathrm{L}}$ is the load capacitance vector of the passive ports.

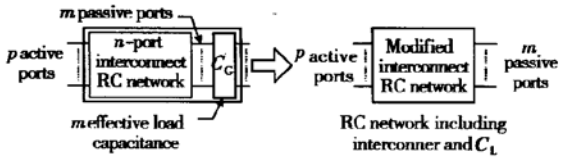

Fig. 2　Network preprocess

We use the Z-parameter to describe the external property of this modified network, and expand it to an n^2-element set.

$$\left\{\frac{V}{I}\right\} = \left\{\frac{v_i}{i_j}\middle| i, j = 1, 2, \cdots, n\right\} \qquad (3)$$

According to the classification of the ports, the Eq. (3) is divided into four non-overlapping subsets.

$$\left\{\frac{V}{I}\right\} = \left\{\frac{V_{\mathrm{act}}}{I_{\mathrm{act}}}\right\} \cup \left\{\frac{V_{\mathrm{pas}}}{I_{\mathrm{act}}}\right\} \cup \left\{\frac{V_{\mathrm{act}}}{I_{\mathrm{pas}}}\right\} \cup \left\{\frac{V_{\mathrm{pas}}}{I_{\mathrm{pas}}}\right\} \qquad (4)$$

here, I_{act} and I_{pas} represent the excitation current vector of the active and passive ports. V_{act} and V_{pas} represent the voltage vector across the corresponding current sources. Since there will no excitations on the passive ports and these ports are open ended in the actual circuits, the last two subsets can be pruned without any affection on the behavior of the whole circuit. That is to say pn of the total n^2 elements is enough to describe the external property in actual circuit.

Thus we can form a new parameter $H'(s)$ to describe the necessary external property of the network by removing the current sources on the passive ports and keeping these ports open ended. Then the inputs are the current sources on the active ports and the outputs are the voltage of total n ports, and $H'(s)$ can be described as the following formulation.

$$H'(s) = B^T(\boldsymbol{G} + s\boldsymbol{C})^{-1}B_{act} \tag{5}$$

Thus the reduction process only need to do the moment matching action on the newly constructed property $H'(s)$, which is a small subset of $H(s)$. In next section, we choose the MPVL method to prove the efficiency of this new model.

3 Model reduction

Here, we choose a general p-input m-output RLC network as the original network and MPVL as the reduction process. First, an expansion point, $s_0 \in \boldsymbol{C}$, is chosen to guarantee $\boldsymbol{G} + s_0\boldsymbol{C}$ nonsingular. So a LU-factorization can be done.

$$\boldsymbol{G} + s_0\boldsymbol{C} = \boldsymbol{F}_1\boldsymbol{F}_2 \tag{6}$$

where $\boldsymbol{F}_1$ is a lower-triangular matrix and $\boldsymbol{F}_2$ is an upper-triangular matrix. Thus, the transfer function can be written in a standard form.

$$H(s) = L^T(I - (s - s_0)A)^{-1}R \tag{7}$$

here, $L = \boldsymbol{F}_2^{-T}E = [w_1\ w_2\ \cdots\ w_n]$, $R = \boldsymbol{F}_1^{-1}B = [v_1\ v_2\ \cdots\ v_n]$ and $A = -\boldsymbol{F}_1^{-1}\boldsymbol{C}\boldsymbol{F}_2^{-1}$. Expanding $H(s)$ about s_0 gives

$$H(s) = \sum_{i=0}^{\infty} M_i(s - s_0)^i \tag{8}$$

here, the coefficients, $M_i = L^TA^iR$, are called moments of $H(s)$. In the MPVL process, the moments are obtained by generating Krylov subspace. The left and right Krylov subspace generated by a k-iteration MPVL process are shown as Eqs. (9) and (10).

$$\mathrm{Kr}(A, L, k) = \mathrm{colsp}[L^T, L^TA, \ldots, L^TA^{a-1}, w_1^TA^a, \ldots, w_b^TA^a]$$
$$\text{where}\quad a = \lfloor k/m \rfloor,\quad b = k - am \tag{9}$$

$$\mathrm{Kr}(A, R, k) = \mathrm{colsp}[R, AR, \ldots, A^{c-1}R, A^cv_1, \ldots, A^cv_d]$$
$$\text{where}\quad c = \lfloor k/p \rfloor,\quad d = k - cp \tag{10}$$

From above analysis, we can draw the following conclusion.

Lemma 1: For a p-input m-output time-invariant linear network, if a qth order matching is required,

$$H_q(s) = H(s) + O((s - s_0)^q) \tag{11}$$

then the MPVL iteration k must satisfy following inequality.

$$\left\lfloor \frac{k}{p} \right\rfloor + \left\lfloor \frac{k}{m} \right\rfloor \geqslant q + 1 \tag{12}$$

Proof: We assume a k-iteration MPVL process is applied, and the generated Krylov spaces are as Eqs. (9) and (10). Then we can see that the highest moment vector that matched during this MPVL process is $L^TA^{a+c-1}R$. If a qth order matching is required, the condition $a + c - 1 \geqslant q$ must be satisfied, and so Eq. (12) is got.

For an n-port network (p active ports and m passive port, $n = p + m$), in the old model, it is treated as an n-input n-output network, thus the iteration number k must satisfy $\left\lfloor \frac{k}{n} \right\rfloor + \left\lfloor \frac{k}{n} \right\rfloor \geqslant q + 1$, where q is the required order of moment matching algorithm. While in the new model, it is treated as a p-input n-output network. Since p is smaller than n, fewer iterations can achieve the same accuracy compared with the old model.

By a k-iteration MPVL process and matrices transforms, we can get the reduced-order circuit equations in standard form.

$$\hat{H}(s) = \hat{\boldsymbol{E}}^T(\hat{\boldsymbol{G}} + s\hat{\boldsymbol{C}})^{-1}\hat{\boldsymbol{B}} \tag{13}$$

here, the matrices $\hat{\boldsymbol{E}} \in \mathbf{R}^{k\times m}$ and $\hat{\boldsymbol{B}} \in \mathbf{R}^{k\times p}$ consist of ones and zeros. The matrices $\hat{\boldsymbol{G}} \in \mathbf{R}^{k\times k}$ and $\hat{\boldsymbol{C}} \in \mathbf{R}^{k\times k}$ are dense. The dimension of the state-space of the reduced-order network equals k, the iteration number of MPVL process. That is to say, when we convert the state equation into an equivalent linear network, its number of nodes will grow linearly with MPVL iteration k, and the number of linear components will grow with a quadratic rate. Thus, we can see that by using our new model, a smaller reduced-order circuit is got. And this results in greatly improved reduction efficiency, especially for those tree-like networks. From Eq. (12) we can also see that when more mo-

ments are needed to be matched, the efficiency of our new model will be higher.

4 Results of experiment

In this section, an equivalent RCL interconnect tree with one input and four outputs is given to prove the efficiency and accuracy of our new interconnect model. This network is driven by a CMOS inverter, and all the outputs are connected with CMOS buffers. The input signal is a ramp voltage source with rise time 0.2ns and voltage amplitude 2V.

Figure 3 shows the simulation results of the original and the reduced-order circuit. We can find that the transient analysis waveform of the 5-iteration MPVL reduced-order circuit by using our new model is almost the same as the result of the original circuit. While using the old model, 15-iteration MPVL process is needed to achieve the same accuracy. The nodes and linear components of reduced-order circuit by using the new model are about 1/3 and 1/9 of that by using the old model, respectively.

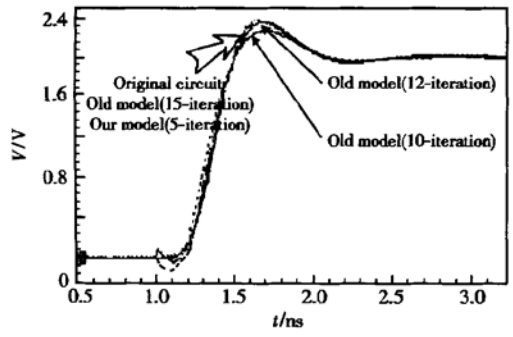

Fig. 3　Transient analysis results of HSPICE

Table 1 shows the reduction results of a 50-ports RC network of different number active ports assumptions. The original network consists of 3264 internal nodes, 3363 resistors, and 3315 capacitors. MPVL approximation matching the first four moments is performed to this network. We can see that if the network only has 10 active ports, the new model will have a great advantage in reduction efficiency over the old one, which is equivalent to the 50-active ports assumption in Table 1.

Table 1　Reduction comparison

Active ports	10	20	30	40	50
Passive ports	40	30	20	10	0
Internal nodes	0	30	50	70	100
Non-zero element of G	1320	1495	1760	2124	2600
Non-zero element of C	2500	5610	7988	10777	15050

5 Conclusion

This paper presents a new interconnect network model for reduction. In this new model, ports are divided into two groups: active and passive ports. By this classification, we can then find that for most interconnect network, a majority of proprieties are redundant. The redundant properties are pruned and only the necessary properties are preserved in the reduced-order network. The simulation results show that the new model has a great advantage in reduction efficiency over the old interconnect model.

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一种用于线性网络约简的高效互连线模型*

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摘要: 给出了一种用于线性网络约简的高效互连线模型. 在这个新模型中, 互连线网络的端口被分为有源和无源两类. 通过端口的分类, 部分的冗余特性可以在约简之前被删减. 使用这种模型, 约简后线性网络的规模可以减小 50% 以上.

关键词: 矩匹配; MPVL 过程; 线性网络约简

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