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Principle and Analysis of Novel Gate-Induced Noise in Pixel MOSFET of CMOS Imagers

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Abstract: A detailed principle and a rigorous analysis of a new noise, the gate-induced noise, in pixel MOSFET of CMOS imagers are provided. The gate-induced noise of the MOSFET is more notable in the strong reversion region than that in the subthreshold region when the applied gate voltage is low. However, the applied gate voltage being up to 3V, the gate-induced noise is more notable with the ω/ω_T increasing when the MOSFET operates in the subthreshold region than that in the strong reversion region. Between the photocurrent I_D and the root mean square value of the gated-induced noise, current $\overline{i_d^2}$ presents the relation of $\overline{i_d^2} \propto \sqrt{I_D}$ in the saturation region of the strong reversion and approximately $\overline{i_d^2} \propto I_D$ in the subthreshold region. A detailed and rigorous study of the gate-induced noise in the reset MOSFET for the photodiode APS and improved photodiode APS are provided. The improvement of logarithmic response APS is analyzed and the simulation results show that the gate-induced noise can be reduced.

Key words: gate-induced noise; pixel MOSFET; improved photodiode APS; CMOS imagers
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1 Introduction

All kinds of noise, such as thermal noise, fixed pattern noise, shot noise, and $1/f$ noise, have set the fundamental limit in the design of analog circuits such as bias circuits and readout circuit of CMOS image sensor[1,2], especially under low frequency linear analog circuits[2]. The noise is undesirable and fluctuating information at random shown by current, voltage or charge[3,4]. This paper presents a new noise, the gate-induced noise in pixel MOSFET of CMOS imagers, which sets one of the fundamental limits on high performance CMOS image sensor, especially under low illumination. When MOSFETs are scaled into deep submicron regime[5], the gate oxide thickness will be reduced. When the thin gate oxide thickness, for example, is below 3nm, the gate-induced noise will result in the direct tunneling current.

The active pixel sensor has become mainstreams in the design of CMOS image sensor because it has more quantum efficiency, lower FPN, and larger dynamic range than the passive pixel sensor[6]. The standard photodiode for CMOS active pixel sensor (CMOS APS), the three-transistor-photodiode pixel[7,8], is shown schematically in Fig. 1. Each pixel contains a photodiode D, a reset transistor M1, a source follower transistor M2, and a read transistor

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M3. The standard photodiode APS reads out one row at a time. At the end of each row's integration time, the pixel values are stored in the column capacitors. Then the row is reset and the stored pixel values are read out via the column multiplexer. During one read-out circle, the M1 in the pixel is reset and the stored pixel values at the node A capacitor are read out via M2 by the way of the logarithm integration. Finally the read M3 is set to a high voltage and the read circle of the pixel values is finished.

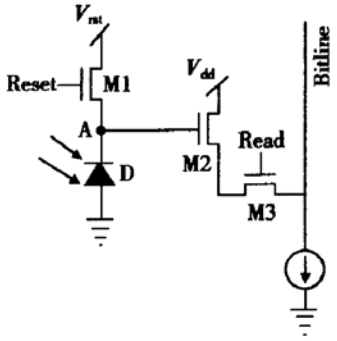

Fig. 1 Standard photodiode CMOS APS circuit

Because the M1, M2, and M3 are in the same pixel cell exposed in the light circumstance, those transistors are easy to be subjected by the incidence light when the CMOS imager operates. When the light shows on the operating chip, the photoelectrons may be excited in the polysilicon gate of MOSFET device and then bring about the gate-induced noise, which will beget the gate voltage's fluctuation so as to result in the channel current's fluctuation via the gate capacitance. Moreover the radicalization from the environment and the variation from low temperature to high temperature also excite excess electrons in the polysilicon gate of MOSFET devices.

2 Principle and analysis of gate-induced noise

2.1 Gate-induced noise model

The excited photoelectrons when the light shows on MOSFET device, and the excess electrons due to the radicalization from the environment and changeable temperature, will beget the gate voltage's fluctuation so as to result in the channel current's fluctuation via the gate capacitance. We define the root mean square value of the noise current $\overline{i_d^2}$ as the magnitude of the gate-induced noise. The $\overline{i_d^2}$ obeys the noise power density function

$$\overline{i_d^2} = S_I(f)\,\Delta f \tag{1}$$

where Δf is the testing bandwidth; $S_I(f) = 4kT\gamma g_{ms}$ is the power spectrum density of the fluctuation i in the unit bandwidth around the frequency f; γ (= 1 when in the linearity region, = 2/3 when in the saturation region) with an infinitude measurement factor reflects the influence of the channel thermal noise due to the underlay deflection effect; g_{ms} is the saturation stride.

Assumed that the gate voltage varies with ΔV_G, the inducing charges ΔQ_n in the MOSFET channel are equal to the gate charges with the opposite symbol by the coupling of the gate-source capacitance C_{gs}.

$$\overline{\Delta Q_n^2} = C_{gs}^2\,\overline{\Delta V_G^2} \tag{2}$$

where $C_{gs} = C_{ox}WL$ is the total gate-source capacitance.

The $\overline{i_d^2}$ results from the fluctuation of the channel barrier distribution, which varies with the change of the channel. On the assumption that the electric field on some spots in the MOSFET channel is a constant, the $\overline{i_d^2}$ satisfies the following formula relative to the channel inducing charges ΔQ_n,

$$\overline{i_d^2} = \overline{(j\omega\Delta Q_n)^2} \tag{3}$$

where ω is the angle frequency.

The formula (2) is substituted for the formula (3),

$$\overline{i_d^2} = \omega^2 C_{gs}^2\,\overline{\Delta V_G^2} \tag{4}$$

On the other hand, the gate voltage fluctuation ΔV_G results in the drain-source current's variation. If both ΔV_G and i_d approximately meet the small signal current-voltage relation, therefore

$$\overline{i_d^2} = \overline{(g_m\Delta V_G)^2} \tag{5}$$

The formula (1) substitutes for formulas (4) and (5), and the MOSFET cut-off frequency is $\omega_T = g_{ms}/g_s$.

$$\overline{i_d^2} = 4kT\gamma\Delta f g_{ms}\left(\frac{\omega}{\omega_T}\right)^2 \tag{6}$$

And the $S_I(f) = \overline{i_d^2}/\Delta f$ denotes the noise frequency chart changing with the frequency f, therefore

$$S_I(f) = 4kT\gamma g_{ms}\left(\frac{\omega}{\omega_T}\right)^2 \qquad (7)$$

2.2 Analysis of gate-induced noise

2.2.1 MOSFET operation in saturation region of strong reversion.

Ignored the influence of the underlay resistance rate and the cascade drain-source resistance, in the saturation region the MOSFET transconductance, g_{ms}, is equal to

$$g_{ms} = \frac{u_n w C_{ox}}{L}(V_G - V_T) \qquad (8)$$

Figure 2 shows that the average square value $\sqrt{S_I(f)}$ is relative to the ω/ω_T and the $V_G - V_T$ when the MOSFET operates in the saturation region of the strong reversion under the consideration of $W/L = 1$, $C_{ox} = 3.45 \times 10^{-2}$F/cm^2 and $T = 300$K.

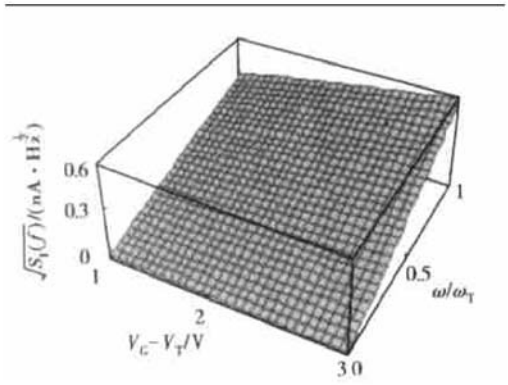

Fig. 2　$\sqrt{S_I(f)}$ versus both ω/ω_T and $V_G - V_T$ when MOSFET operating in saturation region of strong reversion

2.2.2 MOSFET operation in saturation region of weak reversion($V_{DS} \geqslant 3V_{th}$)

The MOSFET transconductance, g_{ms}, in the weak region is as following,

$$g_{ms} = \frac{W}{L} \times I_{D0} \times \frac{1}{nV_{th}} \exp[(V_G - V_T)/nV_{th}] \qquad (9)$$

where $V_{th} = kT/q$, $k(= 1.381 \times 10^{-23}$J/K) is Boltzmann constant; T is the absolute temperature; $q(= 1.6 \times 10^{-19}$C) is the charge; I_{D0} and n are technology parameters and their typical values are $I_{D0} \approx 20$nA and $n = 2$. At the room temperature, V_{th} is 26mV. Figure 3 shows that the average square value $\sqrt{S_I(f)}$ is relative to ω/ω_T and the $V_G - V_T$ when the MOSFET operates in the saturation region of the weak reversion under the consideration of $W/L = 1$ and $T = 300$K.

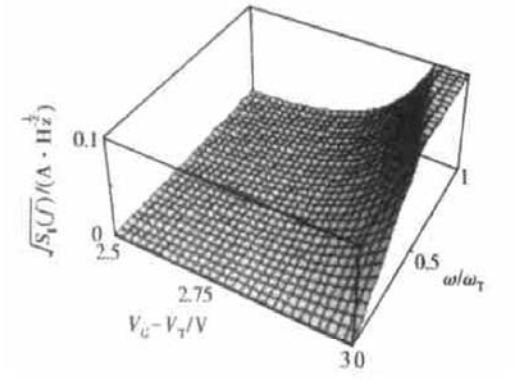

Fig. 3　$\sqrt{S_I(f)}$ versus both ω/ω_T and $V_G - V_T$ when the MOSFET operating in saturation region of weak reversion

When the working frequency of the MOSFET device is a constant, the gate-induced noise of the MOSFET is bigger in the strong reversion region than that in the subthreshold region under the lower gate voltage. As the applied gate voltage goes up, the gate-induced noise of the MOSFET operating in the subthreshold region ascends in term of the exponential law. On the other hand, the applied gate voltage being up to 3V, the gate-induced noise is more noticeable with the ω/ω_T increasing when the MOSFET operates in the subthreshold region than that in the strong reversion region. This is because the saturation transconductance, g_{ms}, is linear in the strong reversion region, but exponential in the subthreshold region.

2.3 Relation between photocurrent and gated-inducing noise current

The relation between photocurrent and the gated-inducing noise is deduced as following. The root mean square value of the noise current $\overline{i_d^2}$ satisfies formula (6). Therefore, the $\overline{i_d^2}$ is linear with the g_{ms}.

When the reset MOSFET operates in the saturation region of the strong reversion ($V_D = V_G - V_T$), the I-V relation is following formula (10).

$$I_D = \frac{u_n W C_{ox}}{2L}(V_G - V_T)^2 = \frac{u_n W C_{ox}}{2L} V_D^2 \quad (10)$$

From formulas (8) and (10), we can draw

$$g_{ms} = \sqrt{\frac{2u_n W C_{ox}}{L} I_D} \quad (11)$$

when the reset MOSFET operates in the subthreshold region, the I-V relation is following the equation.

$$I_D = \frac{W}{L} \times I_{D0} \exp[(V_G - V_T)/nV_{th}] \quad (V_{DS} \geqslant 3V_{th}) \quad (12)$$

From formulas (11) and (12), we can draw

$$g_{ms} = \frac{I_D}{nV_{th}} \quad (13)$$

Therefore, from both formulas (6) and (11) or from both formulas (6) and (13), we can respectively draw the same relation between photocurrent I_D and $\overline{i_d^2}$ in the saturation region of the strong reversion or in the subthreshold region. The gated-induced root mean square value of the noise current $\overline{i_d^2}$ and photocurrent I_D presents the relation $\overline{i_d^2} \propto \sqrt{I_D}$ in the saturation region of the strong reversion and approximately linear relation $\overline{i_d^2} \propto I_D$ in the subthreshold region.

3 Analysis of gate-induced noise in reset MOSFET for APS pixel

In this section the gate-induced noise in reset MOSFET for APS pixel is analyzed. An improved logarithmic response APS circuit is provided and analyzed for reducing the gate-induced noise, and the simulation results are given.

3.1 Improvement of photodiode APS circuit

Compared with the standard photodiode APS, a spill transistor M4 is added, which is held at a constant potential of approximately 1.2V, shown in Fig. 4. If the scene dynamic range exceeds the sensor dynamic range, portions of the image will be clipped in either dark or bright regions. The improved photodiode APS circuit can increase the dynamic range of CMOS imagers in Reference[9], which is originally used to improve the dynamic range in CCD pixel. In this paper it can reduce the gate-induced noise.

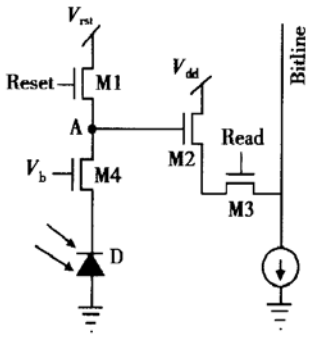

Fig. 4 Improved photodiode APS circuit

3.2 Discussion and simulations

The gate-source capacitor of the gate-induced noise of the photodiode APS or the improved photodiode APS depicted in Figs. 5 (a) and (b) are the feed-through due to the gate to source overlap capacitance. To be simple, an assumption that the equivalent capacitance of the follower transistor M2 has been ignored is taken. In the improved photodiode APS,

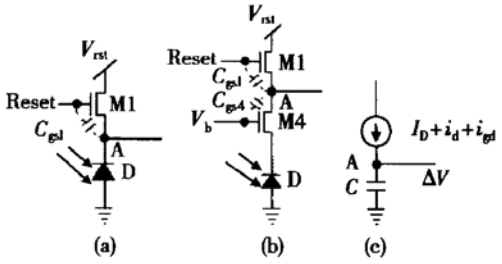

Fig. 5 Diagram of gate-induced noise of photodiode APS or improved photodiode APS and equivalent diagram (a) Photodiode APS; (b) Improved photodiode APS; (c) Equivalent diagram

the equivalent capacitance of the photodiode can be neglected due to the segregating spill transistor M4. In the node A, we can use the equivalent circuit that a current source injects a capacitance where I_D is the photocurrent, i_d is the dark current, and i_{gd} is the gate-induced noise current. There exists a relation as following on the capacitance C,

$$i = C\frac{\partial V}{\partial t} \tag{14}$$

When the i is a constant, the ΔV will decrease as the variety rate $\frac{\partial V}{\partial t}$ is slower, since the capacitance C becomes large and therefore the improved photodiode APS can reduce the gate-induced noise. Due to the Miller affect, the photodiode APS' capacitance at the node A is given by

$$C = C_{gs1} + (1 - A_{v1})C_{gd1} + C_d \tag{15}$$

where A_{v1} is the M1 voltage gain, C_{gs1} is the gate-source capacitance, C_{gd1} is the gate-drain capacitance, and C_d is the equivalent capacitance of the photodiode. On the other hand, the improved photodiode APS' capacitance at the node A equals the Miller capacitance of the M1 and M4 drain-source.

$$C' = C_{gs1} + (1 - A_{v1})C_{gd1} + C_{ds4} + \frac{A_{v4} - 1}{A_{v4}}C_{gd4} \tag{16}$$

where the A_{v4} is the M4 voltage gain, C_{ds4} is the drain-source capacitance, C_{gd4} is the gate-drain capacitance. In general, the typical equivalent capacitance of the photodiode C_d is about 1pF, the typical drain-source capacitance C_{ds4} varies from 0.1pf to 1pF, the gate-drain capacitance C_{gd4} is from 1pF to 10pF and the absolute value of the voltage gain A_{v4} is equal to the multiple of the transcondutance g_{m4} and the output resistor at the node A. The gate-induced noise decreases for formula (14) and then the improved photodiode APS improves the anti-disturbance and sensitivity.

A transient sine voltage source with 1M frequency and 25μV amplitude is applied as the gate voltage's fluctuation. Based on the technology TSMC0.5, the fourier analysis diagram of both standard photodiode APS and improved photodiode APS restraining gate-induced noise has been obtained. From the Fig. 6 the improved photodiode APS restraining the gate-induced noise is better than the quasi-standard photodiode APS.

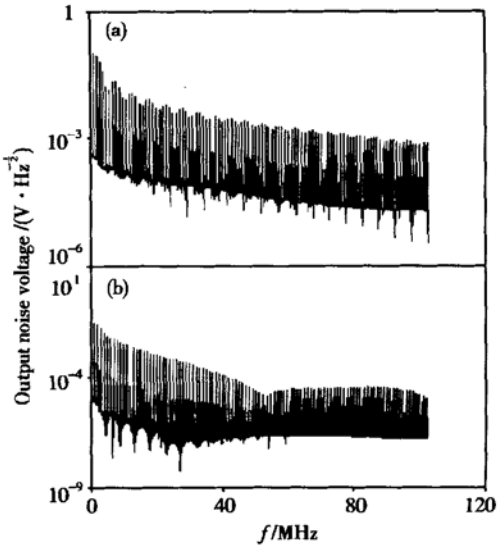

Fig. 6　Fourier analysis diagram　(a) Standard photodiode APS; (b) Improved photodiode APS

4 Conclusion

The paper presents the gate-induced noise and provides a detailed and rigorous principle of the gate-induced noise in pixel MOSFET of CMOS imagers. We can draw some conclusions, which show that the influence of the gate-induced noise is different due to the difference of the working frequency and the applied gate voltage, when the MOSFET is operating in the subthreshold region or in the strong reversion region. The gate-induced noise of the MOSFET is more noticeable in the strong reversion region than that in the subthreshold region when the applied gate voltage is low. However, the applied gate voltage being up to 3V, the gate-induced noise is more noticeable with the ω/ω_T increasing when the MOSFET operates in the subthreshold region than that in the strong reversion region. On the other hand, the gate-induced root mean square value of the noise current $\overline{i_d^2}$ and photocurrent I_D present the relation $\overline{i_d^2} \propto \sqrt{I_D}$ in the saturation region of the strong reversion and approximately linear relation $\overline{i_d^2} \propto I_D$ in the subthreshold region. Appling a transient sine voltage source with 1M frequency and 25μV amplitude substitutes for the gate voltage's fluctuation, the improved photodiode APS restraining the gate-induced noise is lower than the standard pho-

todiode APS.

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CMOS 图像传感器像素中 MOSFET 晶体管的栅感应噪声原理及分析

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摘要: 提出一种 CMOS 图像传感器像素中 MOSFET 晶体管的栅感应噪声原理. 分析表明 MOSFET 工作于强反型区的栅感应噪声比工作于亚阈值区明显, 但当施加在栅极电压达到 3V 时, 随着 ω/ω_T 比值的增加, MOSFET 工作于亚阈值区的栅感应噪声比工作于强反型区明显. 同时详细分析了有源像素(APS)中的 RESET 晶体管的栅感应噪声的影响并提出抑制栅感应噪声的电路.

关键词: 栅感应噪声; 像素 MOSFET; 改进的 APS; CMOS 图像传感器

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