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Progress and Research on Interconnects Crosstalk in Deep Submicron Technology*

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Abstract: As develops in deep sub-micron designs, the interconnect crosstalk becomes much more serious. Especially, the coupling inductance can not be ignored in gigahertz designs. So shield insertion is an efficient technique to reduce the inductive noise. In this paper, the characteristics of on-chip mutual inductance (as well as self) for coplanar, micro-stripline and stripline structures are introduced first. Then base on the coplanar interconnect structures, the effective coupling K_{eff} model and the RLC explicit noise model are proposed respectively. The results of experiments show that these two models both have high fidelity.

Key words: interconnect crosstalk; crosstalk noise; K_{eff} model; RLC explicit noise model
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1 Introduction

It has been shown for years that interconnect delay and crosstalk have become bottle necks in determining circuit performance. Even though most of current research on interconnect synthesis use the RC model, it is evident that the RLC model becomes more appropriate as the on-chip inductive effect gains increasing prominence in gigahertz designs[1] due to the longer wires, shorter rise times, and lower resistive wires. Therefore, modeling and layout optimization for on-chip inductance have been drawing more attention[1].

Characteristic of on-chip self inductance have been studied recently in Ref. [2]. However, without considering mutual inductance, the resulting layout designs might be far away from the optimal. Contrast to Ref. [2], Ref. [3] studies the modeling and layout optimization to minimize the inductive coupling. It first investigates the characteristics of on-chip mutual inductance (as well as self) for coplanar, micro-stripline and stripline structures. With respect to the on-chip inductive coupling, it also examines the impacts of layout design freedoms, such as wire sizing, spacing, and shielding. The characteristic of interconnect structures, especially the coupling, inductance is the foundation of the future work, as we will build models on these structures, and also these models will be used to solve

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crosstalk minimization problems. In this paper, two models considering the coplanar interconnect structures which discussed in Ref. [3] are introduced.

Several previous studies have considered interconnect optimization under the RLC model for multiple coupled nets. In Ref. [4], assuming that current will return from the nearest shield, the loop inductance model is used in Refs. [3, 4, 6]. A formula-based K_{eff} model is proposed in Refs. [3, 9] as the figures of merit for inductive coupling in the three interconnect structures. Using this model, Ref. [4] formulates two simultaneous shield insertion and net ordering (SINO/NB-k and SINO/NF-k) problems and uses SA based algorithm to find a minimal-area SINO solution. Further, it is used to study the min-area simultaneous signal and power routing problem under a given noise bound (the SPR/NB-k problem)[5]. They use capacitive noise and inductive noise computed by K_{eff} model as the noise bound. Although, the assumption is not true in general[1], the K_{eff} model is less intuitive and convenient to the designer comparing to the RLC explicit noise model, and it is easy to compute and keep a high fidelity versus the SPICE-computed RLC noise voltage for SINO solutions.

A current recent article[1] removes the above assumption about the current return path. A table-based partial inductance model[11,12] is adopted without pre-assuming any current return path; additionally, a coupling inductance screening rule[6] is employed to decide the scope of the current return path (i. e., the scope of inductive coupling). Further, different from the K_{eff} model, a high-order RLC circuit model is developed in Ref. [1] to compute the peak noise that can be induced for the victim over all signal patterns of its aggressors. Also, the min-area SINO/NB-v problem is formulated to satisfy the given noise bound in Refs. [1, 8]. And the RLC model is applied to a SA based algorithm for SINO problem[8] and the SPR problem[1]. This model is also further used to study switching pattern generation and switching time alignment, which leads to the worst case crosstalk noise for a quiet victim or a noisy one[10].

2 Three types of interconnect structures

Reference[3] investigates the characteristics of mutual inductance for coplanar, micro-stripline, and stripline structures, and also examines the effectiveness of design freedoms such as wire sizing, spacing, and shielding.

2.1 Coplanar interconnect structure

2.1.1 Characteristic of inductance

The coplanar interconnect structure considers only parallel wires of the same length in the same layer. Figure 1 shows an example of this structure.

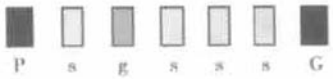

Fig. 1 A cross-section view of a coplanar interconnect structure

In this Figure, P and G represent the power and ground grids (P/G grids), which are often wider than s-wires. S represents the signal wires (denoted as s-wire), and g is a shield wire (in short, a shield), which often has similar width as an s-wire and is directly connected to the P/G grids. Both P/G grids and shield wires provide dedicated current return paths for signals.

An interconnect structure can be represented by a string. The group of s-wires sandwiched by a pair of adjacent g-wires or P/G grids is called as block, and the number of s-wires in a block as the block size. For example, the interconnect structure in Fig. 1 can be represented by gsgsssg (or alternatively, gsg3sg). If the s-wires are labelled from left to right as s_1, s_2, s_3, and s_4, then the string $gs_1gs_2s_3s_4g$ is an unique representation, and the block can be represented as a substring.

2.1.2 Effects of shielding wires

After introducing the structure, Reference[3] studies the coplanar structures with and without

shielding wires respectively. Comparing these two conditions, the effect of shielding on inductance reducing may be concluded.

Firstly, the inductance for the P18sG structure without any g-wire is studied. Referring the experiments in Ref. [3], they suggest the mutual inductance is significant when it compared to the self inductance. Although the mutual inductance decreases for non-adjacent s-wires, it still takes a large scale. Therefore, the mutual inductance between non-adjacent wires can not be ignored, either. Moreover, the loop inductance is not sensitive to the wire sizing and spacing.

Secondly, the inductance for 18 s-wires when g-wires are inserted among them is studied. As shown in Fig. 2[3], when g-wires are inserted, all inductance (both self and mutual) decrease. The more g-wires insert, the less coupling inductanceisare. It also shows that the mutual inductance between adjacent blocks is very small if it is not negligible. Therefore Ref. [3] could assume that the inductive effects are mainly limited inside each block without losing much accuracy.

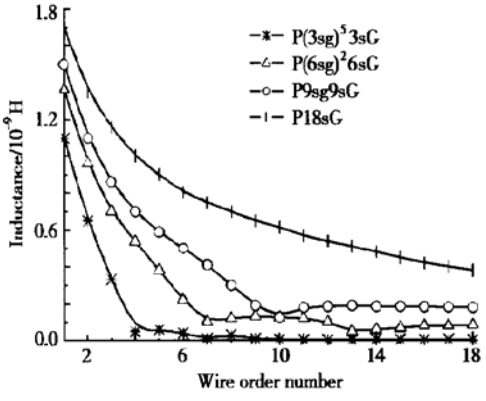

Fig. 2　Self and mutual inductance for wire 1 in four structures

2.2　Stripline and micro-stripline structures

2.2.1　Characteristics of inductance

In the micro-stripline and stripline structures, power/ground planes (in short, P/G planes) are used as current return path for s-wires. A micro-stripline structure is defined when there is only one P/G plane. And a stripline structures is defined when there are two P/G planes. Different from the edge-to-edge space used in coplanar structures, they consider the pitch-space (the center-to-center space) between s-wires[13].

As shown in Fig. 3, if there are n s-wires in a stripline structure, it may be represented by (D_1, ns, D_2), where D_1 (D_2) is the surface-to-surface distance between the lower (upper) P/G plane and the signal layer. Similarly, a micro-stripline with n s-wires can be represented by (D, ns), where D is the surface-to-surface distance between the P/G plane and signal layer in the structure.

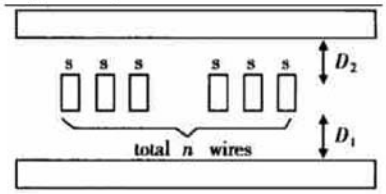

Fig. 3　Cross-section view of stripline structure

2.2.2　Effects of P/G planes

The self and total mutual inductances are all reduced using stripline structures. And also three conclusions may be presented from the experiments in Ref. [3], which uses 0.10μm technology of the strawman technologies[13]. First of all, the more P/G planes are presented, the more self and mutual inductance are reduced. Secondly, as most of the current in s-wires returns from the closest P/G plane, the shielding effect of ground plane is mainly determined by the nearest ground plane. Furthermore, the distance between the P/G plane and the signal layer has great impact on the inductance.

2.2.3　Effects of P/G plane width

Referring to Ref. [3], the micro-stripline structure is used to study the impacts of the P/G plane width. Keeping the micro-stripline structure symmetric, Ref. [3] shrinks the width of plane W, from 200μm to 5μm at a step of 5μm and observes the changes of the mutual inductance between wires.

As shown in Ref. [3], the inductance curve is flat when the P/G plane width is large enough. However, when the P/G plane width is shrunk

close to the total width of the bus structure, the mutual inductances increase quickly.

2.2.4 Effects of wire sizing and spacing

Changing the wire width of the micro-stripline structure to study the impacts of wire sizing and spacing, it is observed in Ref. [14] that mutual loop inductance of two wires is solely decided by the two wires (their lengths, widths and thicknesses, and the spacing between them). Experiments in Ref. [3] further show that the wire width has little impacts on the mutual inductance of two wires in micro-stripline and stripline structures, and mutual inductance mainly depends on the pitch-space between two wires. Therefore, spacing, but not wire sizing, is an effective layout freedom to change mutual inductance.

After the introductions of three types of interconnect structures, the effective coupling model K_{eff} model[3,4] and RLC explicit noise model[1] both considering only coplanar interconnect structures will be described in next two sections respectively.

3 Inductive coupling model

3.1 Sensitivity

Reference[4] defines two net s_1 and s_2 to be sensitive to each other if a switching signal on s_1 will cause s_2 to malfunction or vice-versa. As illustrated in Fig. 4, the aggressor may cause noise in both victim1 and victim2. For victim1, the noise pulse occurs during a sampling window; hence the aggressor and victim1 are sensitive. For victim2, the noise pulse does not occur during a sampling window, hence the aggressor and victim2 are not sensitive and victim2 still works correctly even though there is coupling between the aggressor and victim2.

The sensitivity for all s-wires in a given problem can be represented with a sensitivity matrix $\boldsymbol{S}$ of size $n \times n$ (where n is the number of s-wires) as shown in Fig. 5. The graphical representation of the sensitivity matrix (essentially an undirected graph structure), is also shown in Fig. 5. An entry of {0, 1} in location (i,j) indicates that s_i and s_j are sensitive or not sensitive, respectively, to one another. By definition, the matrix must be symmetric since the underlying graph is undirected (i.e. $s_{ij} = s_{ji}$). By definition, a shield is not sensitive to any s-wire.

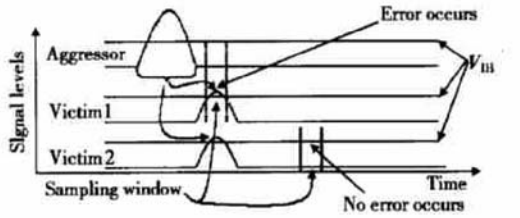

Fig. 4 Illustration of net sensitivity

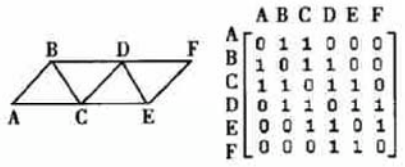

Fig. 5 Illustration of a sensitivity graph and the corresponding sensitivity matrix

3.2 Characteristic of inductive coupling

He *et al.*[4] assume that current will return from shields and therefore they assume a loop inductance model. Under such a model, the characteristics of inductive coupling are illustrated in Fig. 6, which shows the mutual inductance from the leftmost s-wire to all other s-wires. Cases (a) and (b) in the figure show two interconnect structures, g18sg and g6sg6sg6sg, respectively. As shown by (a) where there is no shield between s-wires, the mutual inductance decreases slowly from left to right. In comparing (a) with (b) in the figure, the mutual inductance between wires separated by shields becomes much smaller compared with coupling to wires within the same block. Therefore, shields are effective to reduce inductive coupling.

3.3 Modelling of inductive coupling coefficient

Given the above studies in coplanar interconnect structures, References [3, 4] conclude that compared to wire sizing and spacing, shielding is

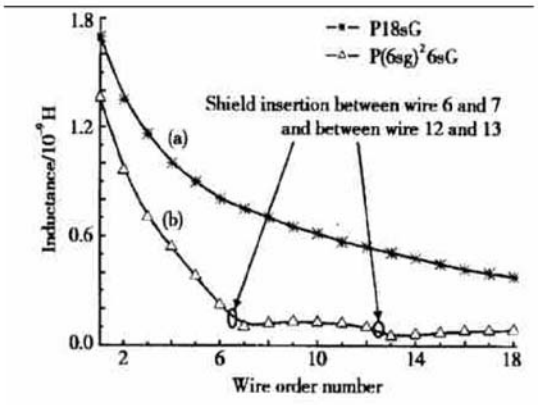

Fig. 6　Illustration of mutual inductive coupling from a signal wire to other signal traces for two coplanar structures

much more effective to reduce inductance, especially mutual inductance. To guide the interconnect structure synthesis using shielding, an effective coupling model will be developed here.

Using the coupling coefficient between two s-wires to characterize the inductive coupling effect between them, the coupling coefficient K_{ij} is defined as:

$$K_{ij} = \frac{L_{ij}}{\sqrt{L_{ii}L_{jj}}} \tag{1}$$

where L_{ii} and L_{jj} is self inductance of wire s_i and s_j, and L_{ij} is mutual inductance between them.

Formula-based K_{eff} model is used to compute the inductive coupling coefficient K_{ij} between two s-wires in Refs. [3, 4]. When s-wires i and j are in different blocks, the coupling coefficient K_{ij} is 0 or a small constant. When they are in the same block, as shown in Fig. 7 where N_iN_j and g_lg_r are track ordering numbers for the two s-wires and g-wires respectively, they consider the following cases for the coupling coefficient computation.

When $i = j$, the mutual inductance is reduced to self inductance and $K_{ii} = 1$ by definition; when N_i(or N_j) becomes g_l(or g_r), because of assuming the loop inductance model with current returning from shields, inductive coupling K_{ij} is between the two segments of the same current loop and is 0 under the loop inductance model; for other general cases, $K_{ij} = K_{ji}$ should be between 0 and 1, and is

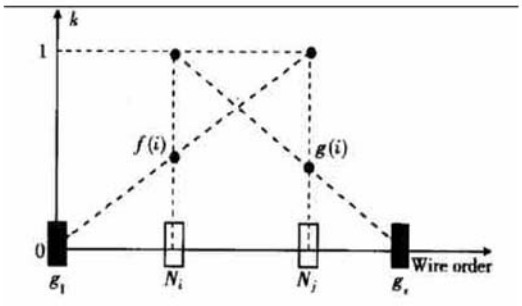

Fig. 7　Illustration of K_{ij} computation

approximated by

$$K_{ij} = \frac{f(i) + g(j)}{2} \tag{2}$$

which is the mean of $f(i)$ and $g(j)$, where $f(i) = \frac{N_i - N_{gl}}{N_j - N_{gl}}$ and $g(j) = \frac{N_{gr} - N_j}{N_{gr} - N_i}$ are two linear interpolation functions. This model for the coupling coefficient is called as effective coupling model, and is denoted as K_{eff} model[3, 4].

It is shown that K_{eff} model is accurate within 15% of numerical extraction, and the higher the K_{eff}, the larger the noise[3]. Based on the K_{eff} model, Reference[4] also defines the effective inductive coupling (in short, K_{eff} model) as

$$K_i = \sum_{j \neq i} S_{ij}K_{ij} \tag{3}$$

where s_j is another s-wire, S_{ij} is the sensitivity between these two s-wires. The K_{eff} model can be used as the figure of merit for the inductive noise that is induced on s_i.

3.4　Experimental verification

In order to verify the accuracy of the formula-based K model, in Fig. 8, Reference[4] generates more than 1000 data points to compare the coupling coefficients given by the formula-based K_{eff} model and FastHenry under different wire widths, thicknesses, lengths, and spacing, as well as different frequencies.

Reference [4] uses coplanar interconnect structures g6sg6sg6sg and g3sg3sg3sg3sg3sg3sg. In Fig. 8, we can observe that all data point essentially fall from the + 20% to − 10% range. There-

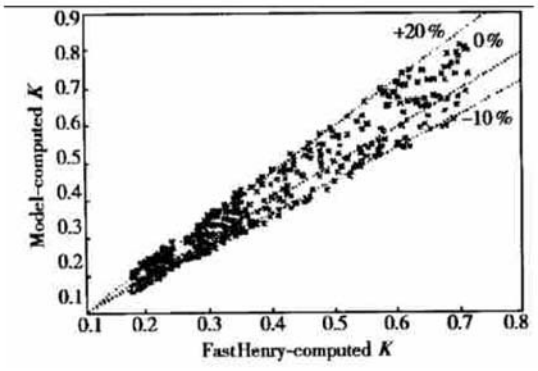

Fig. 8 Comparison of K_{ij} between the K_{eff} model and FastHenry

fore, the formula-based K_{eff} model is reasonably accurate. And it is used extensively in the problem[4] formulations and algorithms.

3.5 Limitation of K_{eff} model

As assuming all current returns via the nearest shields, the K_{eff} model will bring limitation to solving SINO problems. This assumption does not hold in general, as the current may return from quiet wires closer than the nearest shields, and the current may return from quiet wires or shields beyond the nearest shields when multiple wires within a block switch simultaneously. Further, the noise bound in the SINO/NB-k is not an explicit noise voltage that is most useful for the designer. Additionally, the SINO/NF-k and SINO/NB-k problems do not allow placing a victim directly adjacent to an aggressor, and may lead to over design in practice[4].

4 RLC noise modelling

Different from the inductive coupling model, the RLC noise model[11] builds the explicit relationship between the noise and inductive and capacitive coupling coefficients. So the noise bound can be represented as an explicit voltage. RLC explicit noise model does not consider the sensitivity between the s-wires as proposed K_{eff} model above, but use the following definition for the aggressor: s-wire s_i is an aggressor for s-wire s_j if and only if the two wires are sensitive to each other. For a SINO string $s_1s_2gs_3s_4$, if s_1 and s_3 are sensitive to victim s_4, but s_2 is not sensitive to victim s_4, the given SINO string can be also represented as aqqav, meaning that for noise computation, s_1 and s_3 are aggressors for the victim and s_2 as well as the shield are quiet wires for the victim.

The RLC circuit model for coplanar interconnect structures is discussed first, and then does the noise model for coupled RLC interconnects.

4.1 RLC circuit model

In the circuit model, each driver is modeled by a driver resistor R_d, and each receiver by a loading capacitance C_l. A wire is modeled in general by multiple RLC segments. An example of the RLC circuit model for three coupled wires (also called a three-net structure) is given in Fig. 9, where one RLC segment is used for a wire, and R_i, L_i, and C_{gi} (i= 1, 2, and 3) are resistance, self inductance and ground capacitance for the three wires.

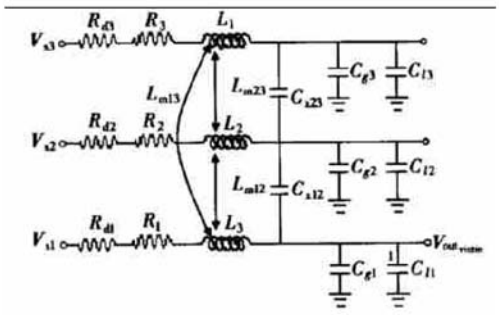

Fig. 9 RLC circuits model for three coupled wires

The coupling capacitance is considered only for adjacent wires, and the coupling inductance is considered for any two wires. In Ref. [1] capacitance and inductance is obtained from interconnect geometry using the table-based models for capacitance and inductance presented in Refs. [11, 15], respectively. As pointed out in Refs. [1, 11, 16], the partial inductance model is used without assuming any current return path in order to achieve an accurate RLC circuit model.

4.2 RLC noise computation

As the coupling inductance is a "long-range" effect, the peak noise for the victim under the RLC circuit model is affected virtually by all aggressors in a coplanar interconnect structure. Even though the one-segment RLC model is used for each wire, the resulting RLC circuit model (called the full model) is still too complicated to be analyzed efficiently for a wide interconnect structure such as a 32-bit bus. A wide interconnect structure is proposed to be decomposed into a number of three-net structures, then the peak noise of the victim is obtained by solving these three-net structures[1].

In the following, referring to Ref. [1], we present a method, in which a wide interconnect structure is converted into many suitable three-net structures to drive the interconnect synthesis. We will also show the discussion on the inductive screening rule to find all aggressors for the given victim.

4.2.1 Circuit model

For each victim under study, the wide interconnect structure is mapped into a number of three-segment RLC circuits in Ref. [1]. Lepak *et al.*[1] use a four-bit bus in Fig. 10 to illustrate the idea, assuming that s_1 is the victim. First, if either the first-order neighbor s_2 or the second-order neighbor s_3 is an aggressor, a three-segment RLC circuit is constructed for s_3, the victim s_1, and its first-order neighbor s_2, using a single segment for each wire. The circuit contains R_i, L_i, and C_i (i= 1, 2, and 3), where R_i is the sum of the resistance of w_i and its driver, L_i is the self inductance of the net, and C_i is the sum of the ground capacitance of w_i and its loading capacitance.

In addition, the circuit has coupling inductances L_{12}, L_{13}, and L_{23}, as well as coupling capacitances C_{12} and C_{23}. Then, if s_4 is an aggressor, another three-segment RLC circuit is constructed for s_4, the victim s_1, and its first-order neighbor s_2, again using a single segment for each wire. Similar

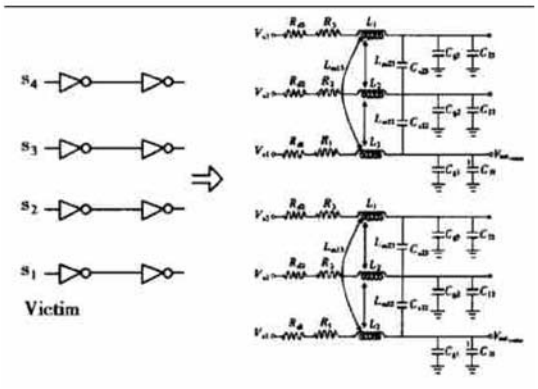

Fig. 10　A four-bit bus is modeled by two three-segment RLC circuits

to the circuit for s_1, s_2 and s_3, the new circuit contains R_i, L_i, and C_i (i= 1, 2, and 4), as well as coupling inductances L_{12}, L_{14}, and L_{24}. However, it has only one coupling capacitance C_{12}. Therefore, the coupling inductance is considered between any two wires, but the coupling capacitance is only considered between the adjacent wires. The inductance and capacitance are computed based on Refs. [11, 15]. An extra three-segment circuit is constructed for every aggressor s_i beyond s_4, considering wires s_1, s_2 and s_i.

4.2.2 Noise for three-segment circuit

Assuming that s_1, s_2, and s_3 are three wires in the three-segment RLC circuit, and s_1 is the quiet victim with noise voltage,

$$V_{\text{victim}} = H_2 V_{s2} + H_3 V_{s3} \tag{4}$$

where V_{s2} and V_{s3} are the input to s_2 and s_3, respectively, and H_2 and H_3 are their transfer functions in the s-domain. Both H_2 and H_3 have the following form,

$$H_{2or3} = \frac{a_0 + a_1 s + a^2 s^2 + a_3 s^3 + a_4 s^4}{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5 + b_6 s^6} \tag{5}$$

A five-pole model is used in Ref. [1] to first solve H_2 and H_3 and then obtain a solution to Eq. (4) using the superposition rule. The coefficients and solution of Eq. (5) can be found in the Appendix of Ref. [1].

4.2.3 Overall noise with inductance screening

The following inductance screening rule is

used to decide the scope of effective aggressors. Let K_s be the screening constant, $W_a(a_i)$ is the accumulative wire width for aggressors between the victim and aggressor a_i (including a_i), and $W_q(a_i)$ is the accumulative wire width for quiet wires or shields between the victim and aggressor a_i (excluding the quiet victim). If $W_a(a_i) \times K_s \leqslant W_q(a_i)$, aggressor a_i does not contribute to the inductive noise induced in the victim. The screening rule is only used for aggressors outside the current block.

4.2.4 Experimental verification

Reference[4] compares the peak noise model according the above algorithm with that generated by SPICE simulation using detailed RLC circuit model. It uses three signal patterns by SPICE simulations, where v is the quiet victim; q can be either a quiet wire with driver and receiver or a shield directly connected to power supply networks as shown in Ref. [4], the model is consistently conservative, with from 7.2% to 51.3% overestimation.

5 Conclusion and future work

In this paper we firstly introduce three interconnect structures. The coplanar structure considering all wires routed in the same layer is used to propose K_{eff} model and RLC noise model. Although, in general the P/G grids, shielding wires, and signal wires will be routed in different layers, the coplanar structure is widely used to global routing layer where all wires are routed. As in deep sub-micron (DSM) designs, the wire thickness is often larger than wire width, and the spacing between adjacent wires is often smaller than the distance between adjacent metal layers. This makes noise in global routing layer larger. If no earlier precautions are taken, the number of failing nets will be very large. Therefore, it becomes increasingly important to consider the crosstalk after global routing. Then the formula-based K_{eff} model and RLC explicit noise model are introduced successively. Although, it is not true in general for K_{eff} model to assume the current return path and it is less intuitive and convenient to the designer compared to the RLC noise model, it is easy to compute and keep a high fidelity versus the SPICE-computed RLC noise voltage for SINO solutions.

Existing works consider the crosstalk minimization after global routing. On one hand, they give the preparation for the detailed routing considering crosstalk. On the other hand, considering the crosstalk in the coplanar interconnects structure may be overabundant. We prospect that the crosstalk minimization in different layers routings will be considered based on the coplanar structure.

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深亚微米工艺下互连线串扰问题的研究与进展*

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摘要：集成电路工艺发展到深亚微米技术后，互连线串扰问题变得越来越严重，尤其在千兆赫兹的设计中，耦合电感的影响不能忽略. 插入屏蔽的操作成为减小耦合电感噪声的有效方法. 文中首先介绍共面、微带状线和带状线三种互连结构下的电感耦合特性，然后分别介绍了基于共面互连结构的用于计算互连线噪声的 K_{eff} 模型和 RLC 精确噪声模型. 实验表明两种模型都有很高的精确度，在解决互连线串扰的物理设计中有广泛的应用.

关键词：互连线串扰；串扰噪声；K_{eff} 模型；RLC 精确噪声模型

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