第 24 卷第 11 期　　半 导 体 学 报　　Vol. 24, No. 11
2003 年 11 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Nov., 2003

Design of 2.5GHz Low Phase Noise CMOS LC-VCO*

Zhang Haiqing and Zhang Qianling

(*ASIC & System State Key Laboratory, Fudan University, Shanghai* 200433, *China*)

Abstract: A 2.5GHz fully integrated LC-VCO is fabricated in a standard single poly 4-metal 0.35μm digital CMOS process, using a complementary cross-coupled topology for lowering power dissipation and reducing the effect of $1/f$ noise. An on-chip LC filtering technique is used to lower the high frequency noise. Accumulation varactors are used to widen frequency tuning. The measured tuning range is 23 percent. A single hexadecagon symmetric on-chip spiral is used with grounded shield pattern to reduce the chip area and maximize the quality factor. A phase noise of -118dBc/Hz at 1MHz offset is measured. The power dissipation is 4mA at V_{DD}= 3.3V.

Key words: 2.5GHz LC-VCO; phase noise; accumulation varactors; on-chip spiral inductor
EEACC: 1230; 1250
CLC number: TN753.9　　**Document code**: A　　**Article ID**: 0253-4177(2003)11-1154-05

1 Introduction

The explosive growth of wireless telecommunication market in the industrial, scientific, medical (ISM) 2.4GHz bands, and the merging of applications of Bluetooth, homeRF, has brought an increasing demands for high-performance radio-frequency circuits in low-cost technologies. At the same time, with the development of sub-micro CMOS process, there are more advantages to integrate the RF circuits with CMOS process.

For commercial applications of Bluetooth and homeRF, single-chip integration of transceiver with standard digital CMOS process is an essential choice for low-cost design. However, a major challenge in the design of systems is the integration of the voltage-controlled oscillator (VCO). There are many factors in digital CMOS process that deteriorate the phase noise performance of VCO. To achieve the low-phase-noise specifications, many trade-offs need to be made among phase-noise, dissipation, chip area and tuning range.

Compared to VCO of other types, LC-VCO is the best choice for the low-phase noise design[1]. The key point to design a low-phase-noise LC-VCO is the design of high-quality inductor and the minimization of device noise of its active circuits. In this work, a fully-integrated LC-VCO is designed and fabricated in a standard 0.35μm digital CMOS process. Many techniques are used to improve the phase noise performance of VCO.

2 Circuit design

2.1 Phase noise

An LC-VCO consists of a lossy resonator and an active circuit across it to overcome this loss. In steady-state, the phase noise sidebands around the oscillation frequency are given by[2]:

* Project supported by National High Technology Research and Development Program of China (No. 2002AA1Z1060)
Zhang Haiqing male, was born in 1972, PhD candidate. His research interests are in RFIC and frequency synthesizer design.
Zhang Qianling, female, was born in 1936, adviser of PhD candidates. Her research interests are in VLSI design.
Received 19 February 2003, revised manuscript received 19 May 2003

$$L\{\omega_m\} = \frac{4FkTR}{V_{RMS}^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \quad (1)$$

where the active circuit noise density is F-1 times the resonator noise, and V_{RMS} is the RMS oscillation amplitude. For a differential LC-VCO in its current-limited operation[2,3], F consists of the following terms arising from the resonator loss, the commutating differential pair, and the current source:

$$F = 1 + \frac{4\gamma RI}{V_0} + \gamma\frac{8}{9}g_{mbias}R \quad (2)$$

where I is the bias current, γ is the transistor noise factor (2/3 for long channels), and g_{mbias} refers to the current source transistor. Two important insights can be obtained from the analysis[2]. Firstly, the phase noise induced by differential pair thermal noise is independent of the specifics of the transistors. Secondly, the noise of current source at frequencies around 2nd harmonic is translated to the oscillation frequency, half of which contributes to the phase noise.

The $1/f$ noise, of which the largest contribution usually comes from the current source, is not considered in the mentioned model. It also affects the phase noise performance of VCO by many kinds of mechanisms[4].

2.2 Optimization of inductor

One of the most important performance parameters for the on-chip spiral is the quality factor Q. It is mainly limited by the loss due to inductor metal resistance, substrate resistance, and that associated with induced eddy current below the inductor metal trace[5,6].

Figure 1 shows the lumped element model for spiral inductors. For the standard single poly 4-metal 0.35μm digital CMOS process, three top metals are used in parallel to reduce the metal serial resistance. The first layer metal is not used to reduce capacitive coupling with substrate. At the same time, the use of patterned ground shield (PGS) between inductor metal trace and substrate increases Q by reducing substrate resistance[6].

Compared to a square spiral inductor with same inductance, the circular spiral inductor has smaller series resistance and parasitic capacitance by a factor of $\pi/4$. Due to the difficulty of implementation, a single hexadecagon symmetrical spiral inductor is designed to reduce the chip area and improve Q.

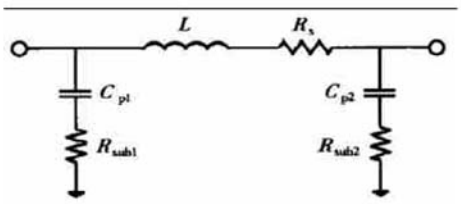

Fig. 1　Lumped element model for spiral inductor

Due to the skin effect and substrate parasitic capacitance, trade-offs must be made for the selection of width and spacing of metal trace.

The simulation tool ASITIC[5] is used to optimize the spiral inductor. The optimized spiral model parameters are given in Table 1.

Table 1　Model parameters of spiral inductor

Q	5.13		
L/nH	5.28		
R_s/Ω	2.05		
R_{sub1}/Ω	0.751	R_{sub2}/Ω	1.15
C_{p1}/fF	85.2	C_{p2}/fF	84.2

2.3 Design of varactors

PMOS transistor can be used as a varactor in digital CMOS process. The tuning of frequency can be achieved by changing the n-well contact voltage. Due to non-monotony of C-V curve of PMOS transistor, the frequency tuning range is not monotonous, making the available tuning range smaller and design of PLL difficult. The accumulation-mode varactor exhibits very good characteristics. Accumulation varactor can be obtained by omitting minority carrier source (P^+) or substituting N^+ diffusion for P^+ diffusion[7,8]. The accumulation varactor has a reasonably uniform capacitance variation over the control voltage range, making the PLL design easier.

In our design, as shown in Fig. 2, a differential inter-digitated layout structure is used with gates

of inverse AC polarity placed very close to each other. Q of varactor is inversely proportional to L_{eff}^2, so the minimum length is used. No N^+ diffusion is interpolated between the sources/drains of varactors to limit the parasitic capacitance by avoiding overlaps.

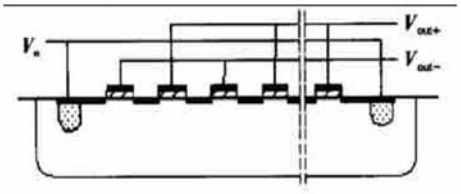

Fig. 2 Accumulation varactor layout

2.4 Design of amplifier

The function of amplifier is to form the positive feedback to eliminate the resonator loss and keep oscillation stable. Figure 3 shows the circuit schematic. A symmetrical complementary structure is used to reduce up-conversion of device $1/f$ noise[9]. In Ref. [9], it is shown that the symmetry of the circuit minimizes the DC coefficient, C_0, of the impulse sensitivity function.

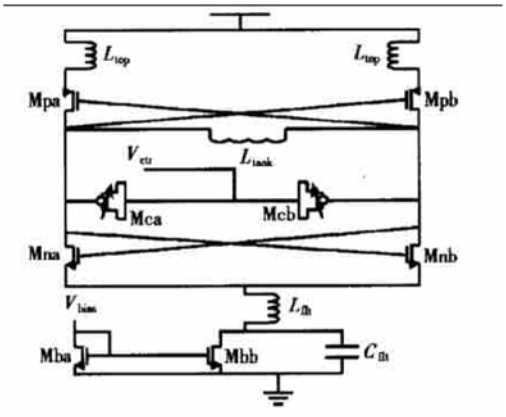

Fig. 3 Complementary structure VCO

The circuit is identical to a cross coupled pair of inverters in parallel to resonator. Because the bias current is used in both PMOS and NMOS devices, twice the negative resistance can be obtained which can reduce circuit dissipation. Another advantage is that its output swing is already at logic level and interfacing to standard CMOS logic is straightforward. The negative resistance seen by resonator is given by

$$R_{\text{negative}} = -\frac{2}{G_{\text{mnmos}} + G_{\text{mpmos}}} \tag{3}$$

As mentioned above analysis, the noise of current source has a large contribution to phase noise of VCO. In order to reduce its effect, an on-chip LC low-pass filter is inserted between current source and commutating transistors to shunt the noise at 2nd harmonic from the current source to ground[3]. Q of the inductor needs not to be high, so only one top metal is used. The capacitance for the filter is implemented with MOS transistor capacitor.

The dimensions of MOS transistors are given in Table 2. The commutating transistors have minimum length to reduce the effect of parasitic capacitance. The channel lengths for current source have larger value to increase its output impedance and eliminate short-channel effect.

Table 2 Design parameters of MOS devices

	Mba, Mbb	Mna, Mnb	Mpa, Mpb	Mca, Mcb
W/L (μm/μm)	2000/0.8	160/0.35	400/0.35	1200/0.35

3 Simulation and experimental results

The die photo is shown in Fig. 4. The chip area without the pads is 0.6mm × 0.5mm, among which the spiral inductor is hexadecagon with the diameter of 0.2mm.

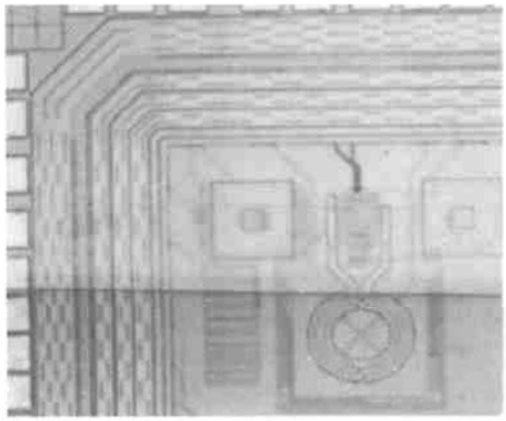

Fig. 4 Die photo of VCO

The operating frequency and phase noise are measured by the measurement setup in Fig. 5.

NMOS open-drain structure is adopted as the output buffer to isolate the VCO core from capacitive loading. External bias-T is connected to the drain nodes of the buffer so that the drain bias of buffer can be provided and output signals can be ac-coupled to the spectrum analyzer.

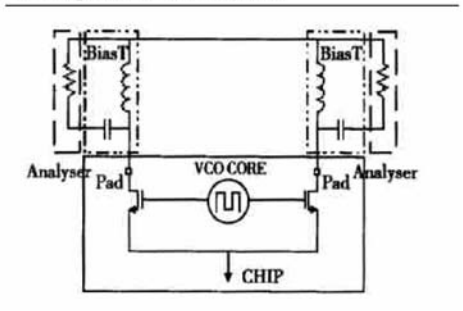

Fig. 5　Measurement setup for VCO

Figure 6 shows the simulation and measurement results of the operating frequency tuning. Simulation and measurement results are in a good match. The operating frequency is between 2.441GHz and 3.031GHz, which corresponds to a tuning range of 23% (the centre frequency as 2.5GHz).

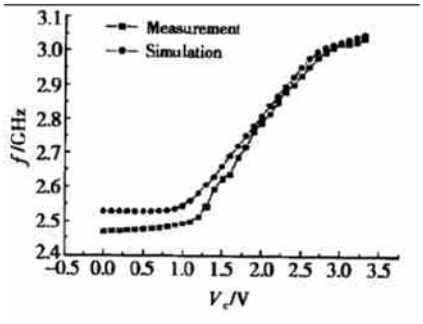

Fig. 6　Simulation and measurement results of operating frequency

Figure 7 is the curve of phase noise of VCO simulated with spectreRF simulator. Because the $1/f$ noise parameters of devices do not be given, its effect on the phase noise is not considered in the simulation and the phase noise curve has a declining slope of - 20dB/dec. The output spectrum measured with spectrum analyzer is shown in Fig. 8 for phase noise measurement. At 2.5668GHz, the phase noise is - 118dBc/Hz at 1MHz frequency offset. The power dissipation is 4mA at V_{DD} = 3.3V. Due to the restriction of experimental condition, the curve of phase noise to offset frequency can not be obtained. At the same time, if more clear power supplies were used, better phase noise results could be achieved.

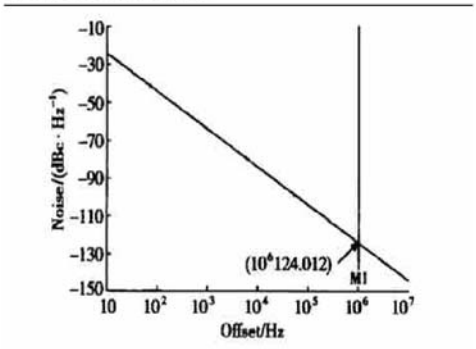

Fig. 7　Phase noise simulation result for VCO

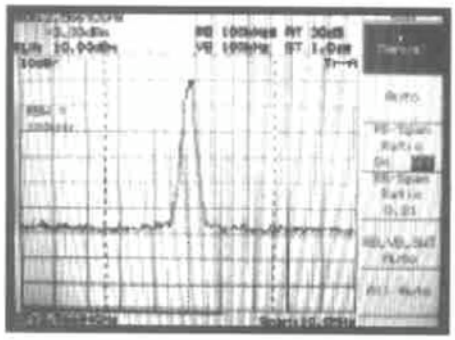

Fig. 8　Phase noise measured spectrum for VCO

4　Conclusion

A 2.5GHz fully integrated LC-VCO is fabricated in a standard single poly 4-metal 0.35μm digital CMOS process, using a complementary cross-coupled topology for lowering power dissipation and reducing the effect of $1/f$ noise. An on-chip LC filtering technique is used to lower high frequency noise. Accumulation varactors are used for the wide frequency tuning. The operating frequency is between 2.441GHz and 3.031GHz for 3.3V power supplies, which corresponds to a tuning range of 23%, and a good tuning linearity is obtained. A single hexadecagon symmetric on-chip spiral is used with grounded shield pattern to reduce the chip area and maximize the quality factor. Three upper metals are used in parallel for inductor trace to re-

duce series resistance loss. A phase noise of - 118dBc/Hz at 1MHz offset is measured. The power dissipation is 4mA at V_{DD}= 3.3V.

Acknowledgement The authors would like to thank Chen zhiqun, Zhang dan and Sun Xiaowei from Shanghai Institute of Microsystem and Information Technology, CAS for their help in circuit measurements; and Shanghai Integrated Circuit Centre for MPW project support.

References

[1] Craninckx J, Steyaert M S. Wireless CMOS frequency synthesizer design. Norwell: Kluwer Academic Publishers, 1998

[2] Rael J J, Abidi A. Physical processes of phase noise in differential LC oscillators. Proc CICC 2000, 2000: 569

[3] Hegazi E, Sjoland H, Abidi A. A filtering technique to lower oscillator phase noise. Proc ISSCC 2001, 2001: 364

[4] Andreani P, Sjoland H. Tail current noise suppression in RF CMOS VCO's. IEEE J Solid-State Circuits, 2002, 37(3): 342

[5] Nguyen N M, Meyer R G. Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's. IEEE J Solid-State Circuits, 1998, 33(10): 1470

[6] Yue C P, Wong S S. On-chip spiral inductors with patterned grounded shields for Si-based RF IC's. IEEE J Solid-State Circuits, 1998, 33(5): 743

[7] Porret A S, Melly T, Enz C C, et al. Design of high-Q varactors for low power wireless applications using a standard CMOS process. IEEE J Solid-State Circuits, 2000, 35(3): 356

[8] Andreani P, Mattisson S. On the use of MOS varactors in RF VCO's. IEEE J Solid-State Circuits, 2000, 35(6): 905

[9] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179

2.5GHz 低相位噪声 CMOS LC VCO 的设计*

张海清 章倩苓

(复旦大学专用集成电路与系统国家重点实验室, 上海 200433)

摘要: 用 0.35μm、一层多晶、四层金属、3.3V 的标准全数字 CMOS 工艺设计了一个全集成的 2.5GHz LC VCO, 电路采用全差分互补负跨导结构以降低电路功耗和减少器件 1/*f* 噪声的影响. 为了减少高频噪声的影响, 采用了在片 LC 滤波技术. 可变电容采用增强型 MOS 可变电容, 取得了 23% 的频率调节范围. 采用单个 16 边形的对称片上螺旋电感, 并在电感下加接地屏蔽层, 从而减少芯片面积, 优化 *Q* 值. 取得了在离中心频率 1MHz 处- 118dBc/Hz 的相位噪声性能. 电源电压为 3.3V 时的功耗为 4mA.

关键词: 2.5GHz LC VCO; 相位噪声; 增强型可变电容; 片上集成螺旋电感

EEACC: 1230; 1250

中图分类号: TN753.9 **文献标识码**: A **文章编号**: 0253-4177(2003)11-1154-05

* 国家高技术研究发展计划资助项目(编号: 2002AA1Z1060)

张海清 男, 1972 年出生, 博士研究生, 主要研究方向为射频电路设计与频率合成器.

章倩苓 女, 1936 年出生, 博士生导师, 主要研究方向为 VLSI 的实现.

2003-02-19 收到, 2003-05-19 定稿