Performance of a Self-Aligned InP/GaInAs SHBT with a Novel T-Shaped Emitter

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Abstract: A self-aligned InP/GaInAs single heterojunction bipolar transistor (HBT) is investigated using a novel T-shaped emitter. A U-shaped emitter layout, selective wet etching, laterally etched undercut, and an air-bridge are applied in this process. The device, which has a 2μm × 12μm U-shaped emitter area, demonstrates a common-emitter DC current gain of 170, an offset voltage of 0.2V, a knee voltage of 0.5V, and an open-base breakdown voltage of over 2V. The HBT exhibits good microwave performance with a current gain cutoff frequency of 85GHz and a maximum oscillation frequency of 72GHz. These results indicate that these InP/InGaAs SHBTs are suitable for low-voltage, low-power, and high-frequency applications.

Key words: self-alignment emitter; InP; single heterojunction bipolar transistor; T-shaped emitter; U-shaped emitter layout
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1 Introduction

InP/InGaAs HBTs are attractive for micro/millimeter-wave and ultrahigh-speed OEIC applications due to their excellent performance. To date, the advantage of the speed of InP-based HBTs has been well demonstrated. The highest current gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) have been achieved with InP HBTs[1~6].

Reducing the base collector capacitance C_{bc} and base resistance r_b of HBTs is the key to improving their performance. Self-alignment technology between the emitter and base electrodes is often used for this purpose. However, it is difficult to prevent self-aligned B-E from shorting because of the crystal orientations. Several techniques can be used to achieve self-alignment, such as selective wet over-etching, ECR or ICP dry etching[7], a T-shaped emitter electrode[8,9], and crystallographically defined emitter contact (CDC) technology[10~12].

As a new way to achieve self-alignment, we have developed a novel T-shaped emitter contact using two-layer dielectric thin film (SiO_2/Si_3N_4). In this experiment, to avoid the influence of B-E shorting, a novel method is used to maintain an acceptable B-E gap. We successfully fabricate a 2μm × 12μm self-aligned InP/InGaAs SHBT that demonstrates good performance.

2 Device structure and fabrication process

2.1 Epitaxial structure

Our epitaxial layers of lattice-matched InP/$Ga_{0.47}In_{0.53}As$ SHBTs were grown on 50mm semi-insulating (100) InP substrate with a V90 gas-source molecular beam epitaxy system at the Shanghai Institute of Microsystem and Information Technology of the Chinese Academy of Sciences, and the devices were fabricated at the Compound Semiconductor Device Department of the Institute of Microelectronics at the Chinese Academy of Sciences.

Group-V arsenic and phosphorus beams are obtained by the thermal cracking of arsine (AsH_3) and phosphine (PH_3) at high temperatures. 7N-purity ele-

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mental gallium (Ga) and indium (In) are used as the group-III sources. Silicon (Si) and beryllium (Be) are used for n- and p-type dopants, respectively[13]. The structure is shown in Table 1. This is a typical structure for an InP/ $Ga_{0.47}In_{0.53}As$ SHBT. The 5nm undoped $Ga_{0.47}In_{0.53}As$ between the emitter and base layers is to prevent the p-type Be-dopant from diffusing into the emitter layer. The 20nm Si-doped InP layer in the sub-collector is an etching-stop layer. The highly doped ($3.5\times10^{19}cm^{-3}$ Be) $Ga_{0.47}In_{0.53}As$ base layer reduces the base resistance and improves the microwave performance.

Table 1　Epitaxial structure of InP/ $Ga_{0.47}In_{0.53}As$ SHBT

Layer	Material	Thickness/nm	Doping/cm^{-3}
Emitter contact	$Ga_{0.47}In_{0.53}As$	150	2×10^{19}
Emitter cap	InP	50	1×10^{19}
Emitter	InP	100	5×10^{17}
Spacer	$Ga_{0.47}In_{0.53}As$	5	Undoped
Base	$Ga_{0.47}In_{0.53}As$	55	3.5×10^{19}
Collector	$Ga_{0.47}In_{0.53}As$	600	2×10^{16}
Sub-collector	$Ga_{0.47}In_{0.53}As$	50	1×10^{19}
	InP	20	1×10^{19}
	$Ga_{0.47}In_{0.53}As$	400	1×10^{19}
(100) InP SI substrate			

2.2　Fabrication

Conventional emitter-up InP HBT devices are fabricated with a standard triple-mesa isolation process. For achieving a self-aligned base-emitter, a T-shaped emitter electrode and selective wet etching are used.

In our experiment, a two-layer dielectric thin film (SiO_2/Si_3N_4) was first deposited on the surface of the cleaned epi-wafer using plasma-enhanced chemical vapor deposition (PECVD). After the U-shaped emitter pattern[14] was defined by contact photo-lithography, the exposed dielectric film was removed with a reactive ion etching (RIE) system to reveal the emitter contact layer. Then, the emitter metal Ti/Au was deposited and lifted off. Next, the dielectric film around the emitter metal was also removed by RIE to obtain the overhanging pattern. A cross-sectional SEM image of the T-shaped emitter electrode is shown in Fig. 1 (Figure 2 is a map of the process). Considering the selectiveness of different etching solutions for semiconductor layers, we chose H_2O_2/citric acid/H_2O and HCl : H_3PO_4 etching solution as the etchants of the $Ga_{0.47}In_{0.53}As$ emitter contact layer and the InP emitter layer, respectively. Ti/Pt/Au and Ti/Au layers were used for the base and collector Ohmic contact metals, respectively. Finally, coplanar pads were connected to the emitter, base, and collector metallization by air-bridge technology.

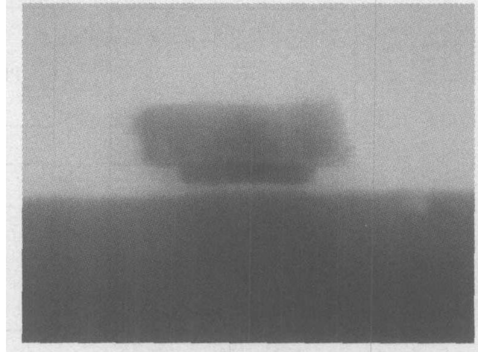

Fig. 1　Cross-sectional SEM image of T-shaped emitter electrode

3　Results and discussion

3.1　DC characteristics

The DC characteristics of the HBT are measured by an HP4155A parameter analyzer. Figure 3 shows the common-emitter DC characteristics of the InP/InGaAs SHBT, which has a $2\mu m\times12\mu m$ emitter area. The peak current gain is over 170. The InP/InGaAs SHBT clearly shows a low offset voltage V_{offset} of approximate 0.2V. The knee voltage V_{knee} is about 0.5V at $I_c=7mA$ and is affected by the parasitic collector resistance. The breakdown voltage BV_{ceo} is over 2V at a $10\mu A$ reverse current. The ideality factors for base and collector current are $n_b=1.28$ and $n_c=1.85$, respectively. These results indicate that the InP/InGaAs SHBTs fabricated in this work are suitable for low-voltage and low-power applications.

3.2　RF performance

The small signal S parameters of the InP/InGaAs SHBT are measured on-wafer by using an HP8510C network analyzer. The current gain h_{21} and maximum available gain (MAG) of the device are shown in Fig. 4. f_T and f_{max} can be extrapolated by extending the curves at the -20dB/decade line. From Fig. 4, f_T and f_{max} of the InP/InGaAs SHBT with a $2\mu m\times12\mu m$ emitter area are found to be 85 and 72GHz, respectively, at a measured point of $V_{ce}=1V$ and $I_c=20mA$. Clearly, f_{max} is below f_T. The reason is that the p-type ohmic contact of the base

is located on the 5nm undoped $Ga_{0.47}In_{0.53}As$ spacer layer instead of on the 55nm Be-doped $Ga_{0.47}In_{0.53}As$ base layer surface, leading to a higher base resistance. Minimizing the base resistance or base-collector junction capacitance C_{bc} improves the high frequency performance. The authors consider that scaling down the device size will greatly enhance the HBT performance.

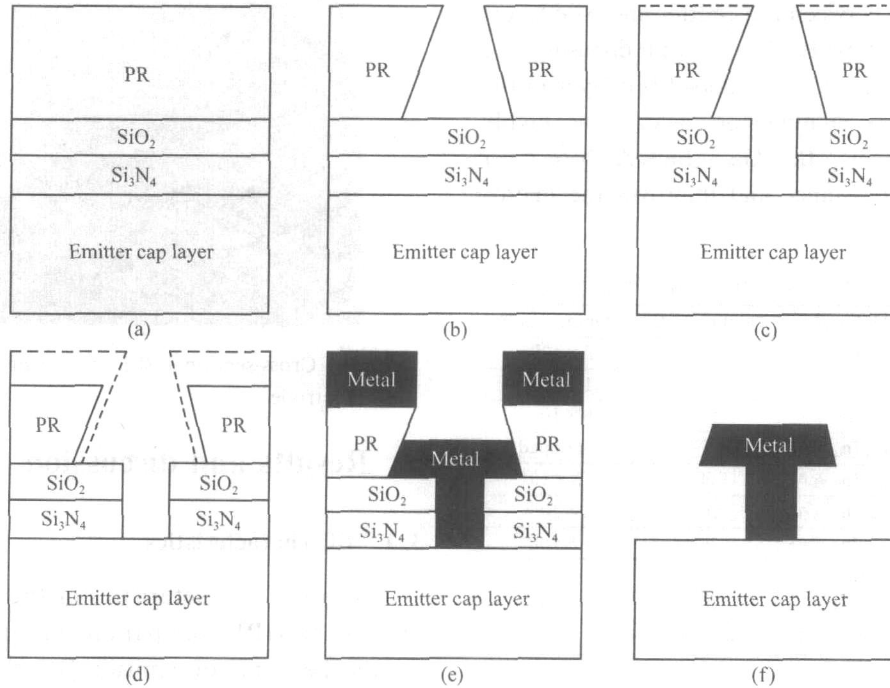

Fig.2 Map of the novel T-shaped emitter fabrication process (a) Deposit dielectric and coat photoresist; (b) Define the emitter pattern; (c) Etch dielectric; (d) Enlarge the pattern window; (e) Evaporate the emitter metal; (f) Lift-off and etch dielectric

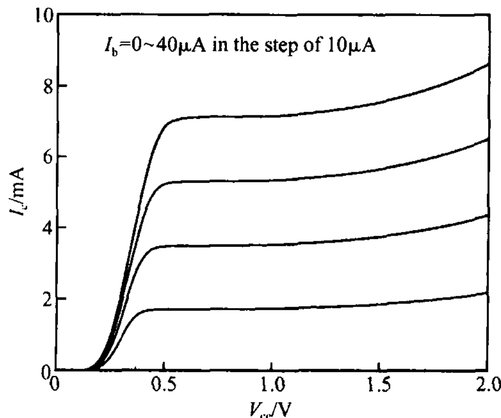

Fig.3 Common-emitter I-V curves of SHBT with a 2μm ×12μm emitter area

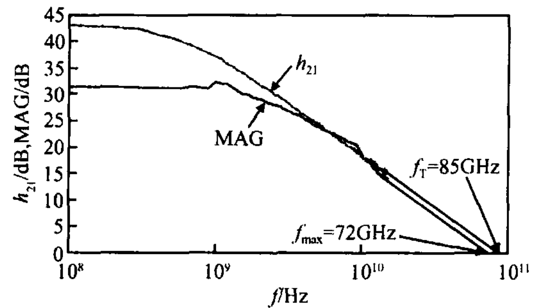

Fig.4 High-frequency performance of 2μm ×12μm InP/InGaAs SHBT at V_{ce} = 1V and I_c = 20mA

4 Conclusion

We have developed a novel T-shaped emitter contact using a two-layer dielectric thin film (SiO_2/Si_3N_4) to manufacture a 2μm ×12μm self-aligned InP/InGaAs SHBT, which shows perfect DC characteristics of $V_{offset} \approx 0.2V$, $V_{knee} \approx 0.5V$, and $BV_{ceo} > 2V$. The devices fabricated here demonstrate good microwave performance with f_T = 85GHz and f_{max} = 72GHz. The above-mentioned results indicate that the devices have great potential in low-voltage, low-power, and high-frequency applications. Optimizing the material growth, device structure, and manufacturing process of the InP/InGaAs SHBT could lead to much higher perform-

ance in future.

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采用新的 T 型发射极技术的自对准 InP/ GaInAs 单异质结双极晶体管的性能

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摘要: 研究了一种采用新的 T 型发射极技术的自对准 InP/ GaInAs 单异质结双极晶体管. 采用了 U 型发射极图形结构、选择性湿法腐蚀、LEU 以及空气桥等技术, 成功制作了 U 型发射极尺寸为 2μm ×12μm 的器件. 该器件的共射直流增益达到 170, 残余电压约为 0.2V, 膝点电压仅为 0.5V, 而击穿电压超过了 2V. 器件的截止频率达到 85GHz, 最大振荡频率为 72GHz, 这些特性使此类器件更适合于低压、低功耗及高频方面的应用.

关键词: 自对准发射极; 磷化铟; 单异质结双极晶体管; T 型发射极; U 型发射极图形
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