Design of a Monolithic CMOS LC-Voltage Controlled Oscillator with Low Phase Noise for 4 GHz Frequency Synthesizers *

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Abstract: A monolithic LC-tuned voltage controlled oscillator (LC-VCO) with 2 tuning terminals is designed for a dual frequency conversion transceiver for WLAN and realized using 0.18μm radio frequency (RF) CMOS technology. The output frequency range can be tuned to cover the defined frequency band of the transceiver. The maximum tuning range is 500MHz. The phase noises are -117dBc/Hz at 4MHz and -107dBc/Hz at 500kHz, both off the center frequency of 4.189GHz. The RMS-jitter of the output signal is 4.423ps, and the output power is -8.68dBm.

Key words: VCO; PLL; WLAN; transceiver
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1 Introduction

Wireless local area network (WLAN) systems have been widely implemented due to the rapid development of information technology and wireless communication. In a WLAN, a series of RF circuits is required for transmitting and receiving signals. A frequency synthesizer is a key part of the transmitter and receiver, which together make up the transceiver, because local oscillating (LO) signals for both the down- and up-conversion mixers are generated by these circuits. A voltage-controlled oscillator (VCO) makes up a core part of the frequency synthesizer. Therefore, the design and realization of a high performance VCO is a key task for transceiver design that is especially challenging to realize with standard CMOS technology.

In this paper, a monolithic LC-VCO realized using 0.18μm RF CMOS technology is discussed. The key components of the circuit and the system aspects related to the architecture and working frequency bands are presented. The circuit techniques related to the VCO are discussed.

2 System aspects

According to WLAN standard IEEE802.11a, three bands are defined between 5.15 and 5.85GHz: 5.15～5.25GHz, 5.25～5.35GHz, and 5.75～5.85GHz[1]. The operation frequency range of the transceiver designed here covers the first two bands, i.e. 5.15～5.35GHz.

For RF transceiver design, several architectures have been developed in history of radio engineering. A well-known one is the super heterodyne.

Figure 1 shows a simplified heterodyne transceiver. In the receiver, the selected RF signal is applied to a low noise amplifier (LNA) and subsequently to an image rejection (IR) filter. The signal is mixed with the signal from local oscillator 1 (LO1), thus the IF signal is produced. After being selected by an IF filter, the IF signal is applied to a down-conversion mixer to obtain the base band signal. The principal issue in heterodyning is the tradeoff between image rejection and adjacent channel suppression. Choosing an appropriate IF and the filters can improve the sensitivity and selectivity of the receiver. Because of multi-conversion stages, the DC offsets and LO leakage can be restrained. The disadvantage of this structure is that both the IR filter and the IF filter require high-Q components that are impractical in today's IC technologies. For this reason, the conventional heterodyne structure is not easily realized on a single chip.

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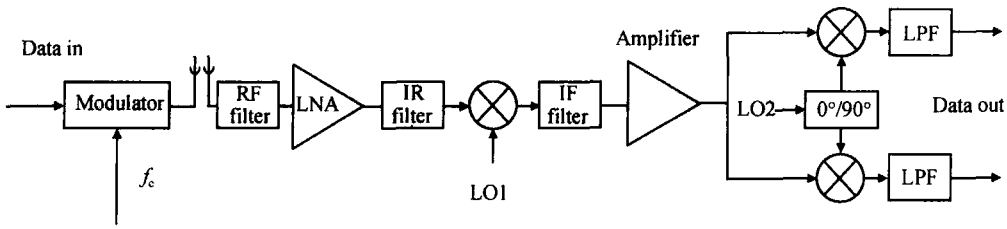

Fig. 1 Simplified heterodyne transceiver architecture

The other architecture is direct-conversion, called zero-IF or homodyne conversion. Figure 2 shows a simplified structure of a zero-IF transceiver. The circuit up to the LNA is the same as that in Fig. 1. Then, the RF signal is mixed with two LO signals in quadrature. Because the LO signals have the same frequency as the RF signal, the base band is obtained directly after mixing. Further, the base band signal is applied to a low pass filter (LPF) and a base-band amplifier. In this structure, the image problem is circumvented because the IF is zero. Both the IR filter and the IF filter can be cancelled. Thus, it is more easily realized in an IC form. However, there is a DC offset problem. The reason is that the RF and LO leakage through the mixer causes the self-mixing and generates DC components.

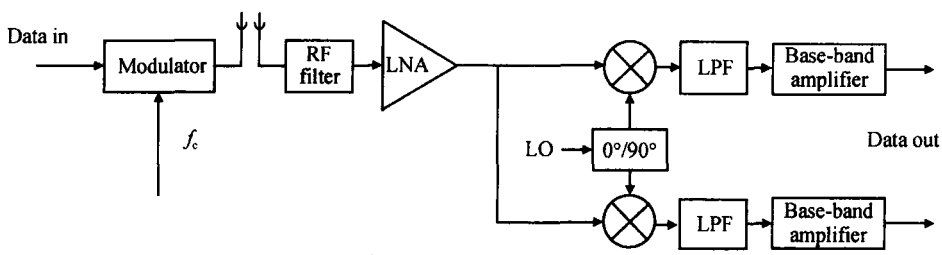

Fig. 2 Simplified zero IF transceiver architecture

We propose a modified architecture of the transceiver shown in Fig. 3. The RF signal from the LNA is first applied to the mixer with the first local oscillator (f_{LO1}) at 4 GHz, which converts the RF signal from 5 to 1 GHz. Then, the 1 GHz RF signal is processed as in a zero IF transceiver.

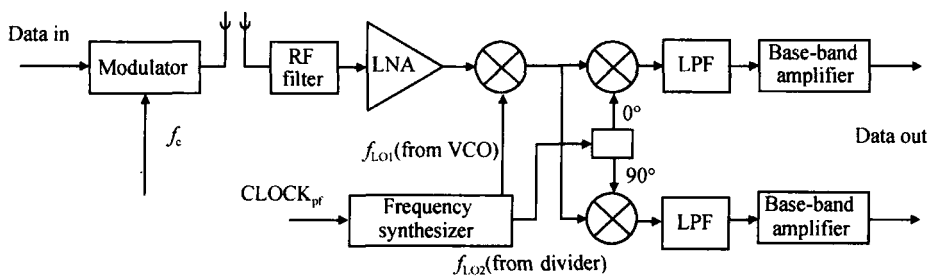

Fig. 3 Simplified dual frequency conversion transceiver architecture

Unlike the conventional heterodyne transceiver architecture, the frequency of the first local oscillator is 4 GHz. Thus, two signals will be produced by the first mixer: One is at 9 GHz; the other is at the desired frequency of 1 GHz. Since the frequency difference of the two signals is so large, the former can be eliminated more easily by the low-pass function of the subsequent stage. The complex IR filter in Fig. 1 is no longer necessary. The problems of the DC offset and LO leakage in the zero-IF architecture in Fig. 2 become less critical due to the difference between the RF- and the LO1-signals.

Figure 4 shows a block diagram of the frequency synthesizer in Fig. 3. It is made up of a phase frequency detector (PFD), an LPF, a VCO, and down scalers. The frequency band at 4 GHz is

generated by the VCO, and the frequency band at 1 GHz is obtained by a divide-by-4 divider.

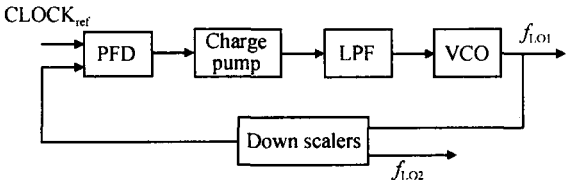

Fig. 4　Block diagram of the frequency synthesizer

The VCO is the key component of the frequency synthesizer. Because $f_{LO1} = 4/5 f_t$ and $f_{LO2} = 1/5 f_t$, the output signal of the VCO should cover the frequency band of 4.1～4.3 GHz.

3 Circuit techniques

The choice of topology is the key to circuit design. The schematic of the LC VCO is shown in Fig. 5. It is a cross-coupled difference VCO with two cross-coupled amplifiers in stack. Two tuning terminals are connected to two different control voltages. The LC resonant tank consists of four metal-insulator-metal (MIM) capacitors, two metal-oxide-semiconductor (MOS) varactors, and an on-chip spiral inductor.

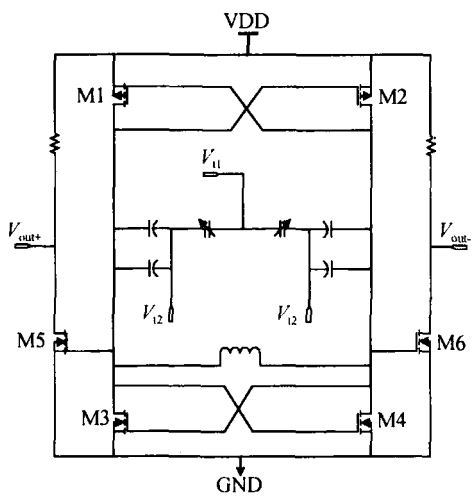

Fig. 5　Circuit schematic of the VCO

As shown in Fig. 5, two crossed-coupled amplifiers providing negative resistance compensate the loss in the LC resonator[4]. One is made up of two nMOS; the other is made up of two pMOS. The total negative resistance is the sum of the the negative resistance of the transistors M1/M2 and that of transistors M3/M4. It can be expressed as

$$-R = \frac{2}{g_{m1,2} + g_{m3,4}} \tag{1}$$

where $g_{m1,2}$ and $g_{m3,4}$ are the trans-conductances of transistors M1/M2 and M3/M4, respectively.

An important parameter of a VCO is the phase noise in the vicinity of the center frequency f_o. The output phase noise at an offset Δf from f_o can be calculated by

$$L\{\Delta f\} = kT(1 + A) Z_o \frac{1}{Q}\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{V_{rms}^2} \tag{2}$$

where k is Boltzman's constant, T is the absolute temperature, A is the noise factor safety margin necessary to ensure oscillation start-up, V_{rms} is the root-mean-square voltage at the oscillation node, $Z_0 = (L/C_{total})^{1/2}$ is the characteristic impedance of the LC resonant tank, and Q is the quality factor. This indicates that maximizing the quality factor of the tank circuit would improve the noise performance significantly.

For this circuit design, transistors M1/M2 and M3/M4 can supply currents to each other. Therefore the tail current source can be omitted and the effect of flick noise can be eliminated[5].

The outputs are buffered by two source followers made of M5 and M6. The drain of each transistor is connected to a resistor to provide output matching. In this way the driving ability of the VCO output is enhanced.

The equivalent circuit of the oscillator is shown in Fig. 6. C_{var} is the capacitance of the MOS varactor, and C is that of a MIM capacitor. The whole circuit is made up of an LC resonant tank with a loss and a negative resistance provided by the active devices. The condition for stable oscillation is that the loss in the LC resonant tank must be cancelled by the negative resistance. The oscillation frequency is

$$f_{OSC} = \frac{1}{2\pi\sqrt{L C_{total}}} = \frac{1}{2\pi\sqrt{L\dfrac{CC_{var}}{2C + C_{var}}}} \tag{3}$$

4 Key components

The phase noise is primarily dependent on the quality factor (Q) of the inductor[6～8]. The higher the Q, the lower the phase noise. A Q as high as possible is therefore desired. However, it is very difficult to realize a high-Q inductor on-chip. Several types of inductors are provided by the foundry. But their Q is not high enough at 4 GHz. Therefore

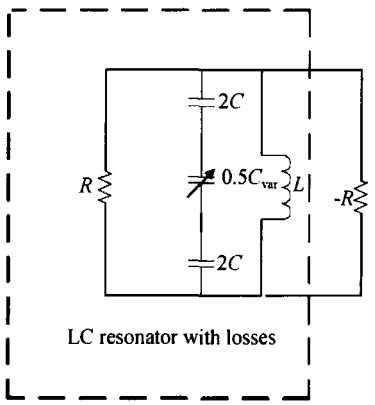

Fig. 6 Equivalent circuit of the oscillator

it is very difficult to get a lower phase noise at 4 GHz with the inductors provided by the foundry.

In order to get a high-Q inductor, a spiral on-chip inductor was designed. All geometric parameters such as the diameter and the number the of turns have been optimized using Momentum, Agilent's electromagnetic analysis program.

A microphotograph of the realized inductor is shown in Fig. 7(a). The inductor with two differential input ports has higher Q than that with a single-ended port at high frequency bands. Because the topology of the VCO circuit is differential, two independent inductors with a single-end port can be replaced by a symmetrical inductor with two input ports. In this way, the chip area can be reduced, and a higher Q can be obtained. The thickest top metal (Metal 6) was selected to form the spiral winding. The trace spacing, width, and the inner dimension are 5, 15, and 80 μm, respectively.

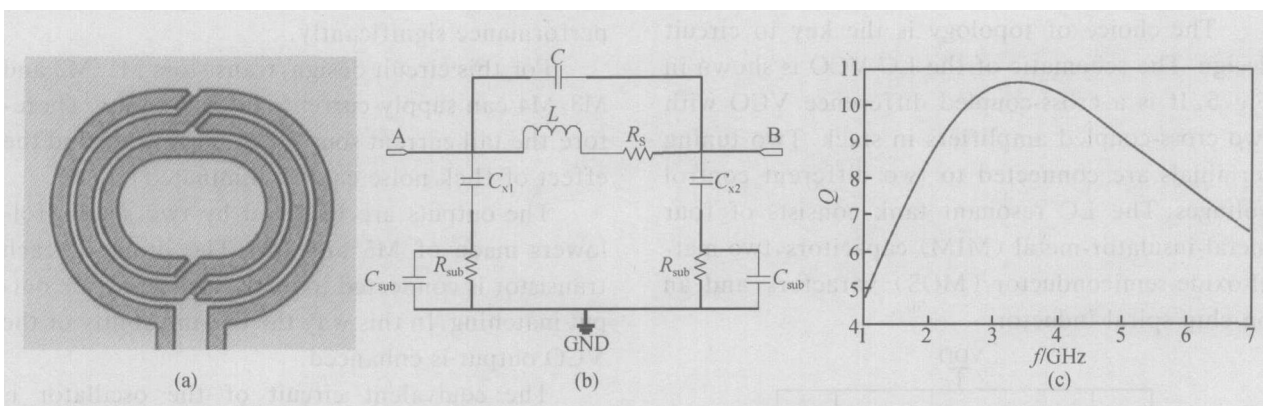

Fig. 7 (a) Microphotograph of the on-chip spiral inductor; (b) Model of the inductor; (c) Q-curve of the inductor

The SPICE model of the inductor is shown in Fig. 7(b). The inductance is about 1.9 nH. Figure 7(c) is the quality curve of the inductor. It shows that the inductor has a $Q > 10$ at 4.2 GHz.

Two types of varactor are provided by the foundry: p^+n type and MOS type. The p^+n type varactor is intended for the frequency band of 1～2 GHz. Thus, it is not suitable for the working frequency bands of our circuit. The MOS type varactor with a low-parasitic resistance and a high Q can be adopted at a higher frequency. Therefore, several MOS varactors have been used in the oscillator. Figure 8 shows a cross-section of such a MOS varactor. It is fabricated in an n well.

Each MOS varactor has 50 branches. Each branch has 2 fingers of the same size on both the drain and the source side. Each finger has a width of 2 μm and a length of 0.5 μm. MOS varactors can

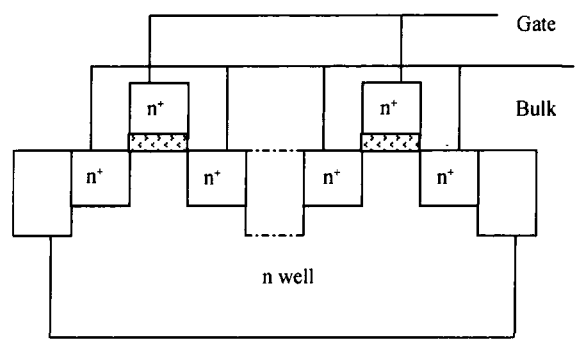

Fig. 8 Cross-section of a MOS varactor

be divided into two types according to the number of fingers. One type has 3 ($g = 3$), and the other has 6 ($g = 6$). The simulation results demonstrated that the tuning range of an oscillator using the former type is too wide. If the tuning range of the VCO is too wide within the same range of the control volt-

age, the VCO gain constant K_{VCO} will become large. In a PLL system, the loop noise can be considerable especially when K_{VCO} is large. Of course, this will cause instability of the loop. Therefore MOS varactors with $g = 6$ have been used in our oscillator. To make frequency band of 4.1 ~ 4.3GHz in the linear region of the tuning curve, two MOS varactors are connected in series as shown in Fig. 5.

The equivalent circuit of the MOS varactor is shown in Fig. 9. The capacitance of the MOS varactor (C_{var}) lies on the voltage between the gate and the bulk. C_{var} is proportional to V_{gate} and inversely proportional to V_{bulk}. With the increase of C_{var}, the oscillation frequency of the VCO decreases. By this characteristic, the gates of the two MOS varactors are connected to the control voltage V_{t1} as the negative tuning terminal, and their bulks are connected to the control voltage V_{t2} as the positive tuning terminal (see Fig. 3). With this structure, a voltage can be generated with a single positive power supply. Thus the tuning range of the VCO is alternated by means of these terminals, and the accuracy of the output signals increases. In the frequency synthesizer, the terminal of V_{t2} is connected to the output of the LPF on the printed circuit board (PCB), and the terminal of V_{t1} is connected to an adjustable control voltage from the outside. In the actual layout design, the terminals of the two MOS varactors are connected to the control voltage terminals respectively to obtain a symmetric layout structure.

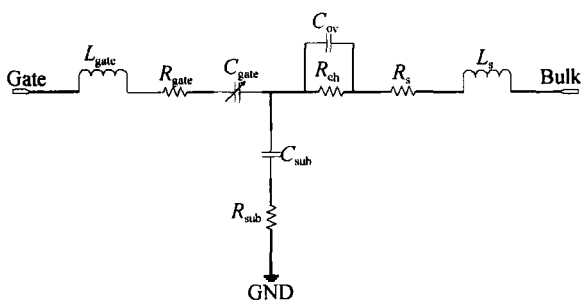

Fig. 9　Equivalent circuit of a MOS varactor

In order to increase the accuracy of the tuning range of the VCO and place the frequency band of the system in the linear region of the tuning characteristic curve, some capacitors with fixed capacitance were added into the LC resonant tank. A square-type MIM capacitor is provided by the foundry. The layout of the MIM capacitor is shown in Fig. 10. The MIM capacitor has two parallel plates with a thin oxide between them. The relationship between widths of two plate metal edges can be expressed as

$$W_{bottom} = W_{top} + 2 \times 3\mu m \quad (4)$$

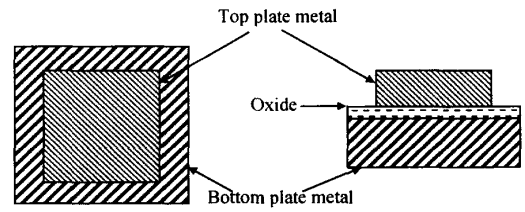

Fig. 10　MIM capacitor layout and cross-section

The width of the top plate is between 10 and 30μm. The capacitance of such a MIM capacitor is determined by the width. Four capacitors with a width of 28μm are used as shown in Fig. 5.

5　IC fabrication and measurement

The VCO circuit was integrated into the frequency synthesizer chip and fabricated in a TSMC 0.18μm CMOS process via MOSIS. The process has 1 poly and 6 metal layers. Figure 11 shows a microphotograph of the realized chip.

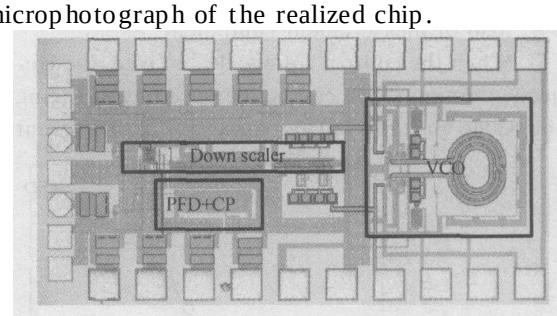

Fig. 11　Microphotograph of the frequency synthesizer chip

The chip consists of three main parts: VCO, PFD + CP, and down scaler. The LPF is off-chip. As the frequency synthesizer is a complex system, enough pads should be put around the core part of the chip for measurement. They are bonded to the PCB with gold wires. Many of the pads are not necessary in the actual transceiver system, and the core part of the chip can be integrated into the transceiver.

Figure 12 shows a photograph of the test PCB. The PCB is fixed onto the ingot by some screws, and the chip is connected with bonding wires to the micro strips at the centre of the PCB. SMA-type microwave

connectors are set at the edge of the box for input and output signals and connected to measurement instruments. With an independent power supply, the VCO can be tested alone. As shown in Fig. 12, the output terminals of the signals from the VCO are on the right side of the PCB.

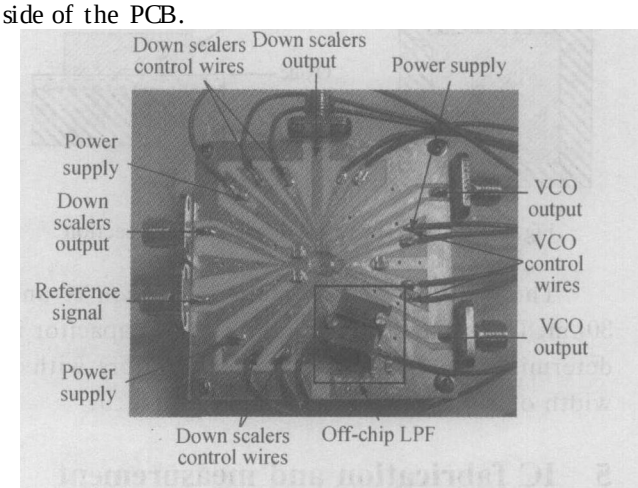

Fig. 12 Photograph of the test PCB

The power supply voltage for the test is 1.8V. The chip draws 16mA from the power supply, 5mA for the VCO core, and 11mA for the output buffers. The output buffer is used to drive a 50Ω load of measurement equipment.

When the control voltage V_{t1} is fixed, the frequency tuning range can be measured by changing the value of the control voltage V_{t2}. Different tuning ranges were got at different values of the control voltage V_{t1}. They are listed in Table 1. From this table it can be seen that as controlled by the V_{t1}, the output frequency of the VCO ranges from 4 to 4.6GHz.

Table 1 Tuning ranges of VCO at different control voltages

V_{t1}/V	f_{low}/GHz	f_{high}/GHz
0	4.1573	4.6392
0.2	4.0801	4.6359
0.4	4.0480	4.6242
0.6	4.040	4.6024
0.8	4.0354	4.5504
1	4.0329	4.5292
1.2	4.0329	4.4767
1.4	4.0310	4.3964
1.6	4.0327	4.2803
1.8	4.0316	4.1540

The measured tuning characteristics of the VCO with the control voltage V_{t2} = 0.8V and V_{t2} = 1V are shown in Figs. 13(a) and (b), respectively. Notice that the frequency band 4.1～4.3GHz is in the linear region of the curve and the slope of the linear region is not too large, which make this circuit a good choice for integration into frequency synthesizers in WLAN transceivers.

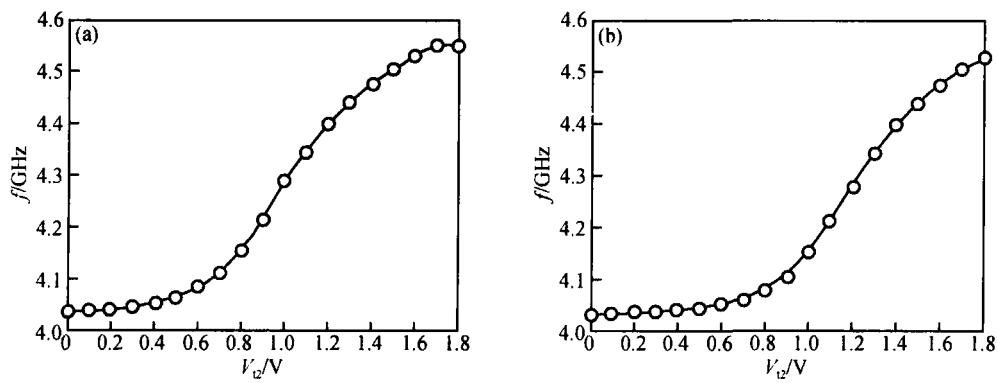

Fig. 13 Measured tuning characteristics of the VCO (a) V_{t1} = 0.8V; (b) V_{t1} = 1V

Figure 14 shows the output spectrum at 4.18871GHz. From Fig. 11(a), it can be seen that the center frequency is 4.1887GHz and the output power is -8.68dBm. The phase noise is -107dBc at 500kHz off the center frequency as shown in Fig. 14(b).

Figure 15(a) shows the output of the VCO in the time domain at the frequency of 4.22GHz in the PLL when the loop is closed. The output jitter is shown in Fig. 15(b). It can be seen in the figure that the jitter time is 4.423ps at the frequency of 4.22GHz.

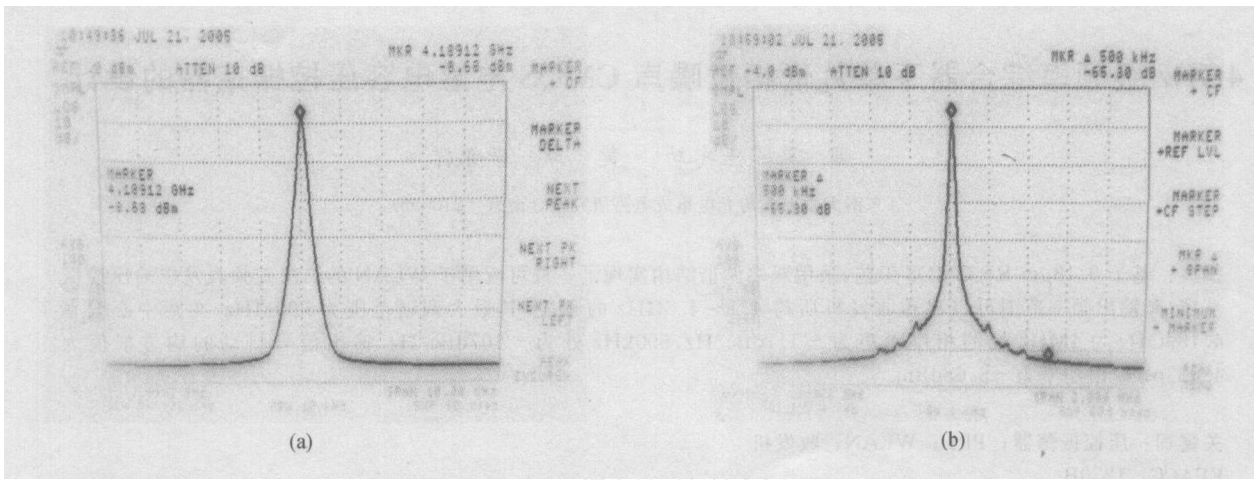

Fig. 14　Spectrum of the 4. 1887GHz output signal　(a) Measured output power (SPAN 10MHz) ; (b) Measured phase noise (SPAN 2MHz ; VBW 1kHz ; RBW 10kHz ; Centre 4. 189GHz ; frequency offset 500kHz)

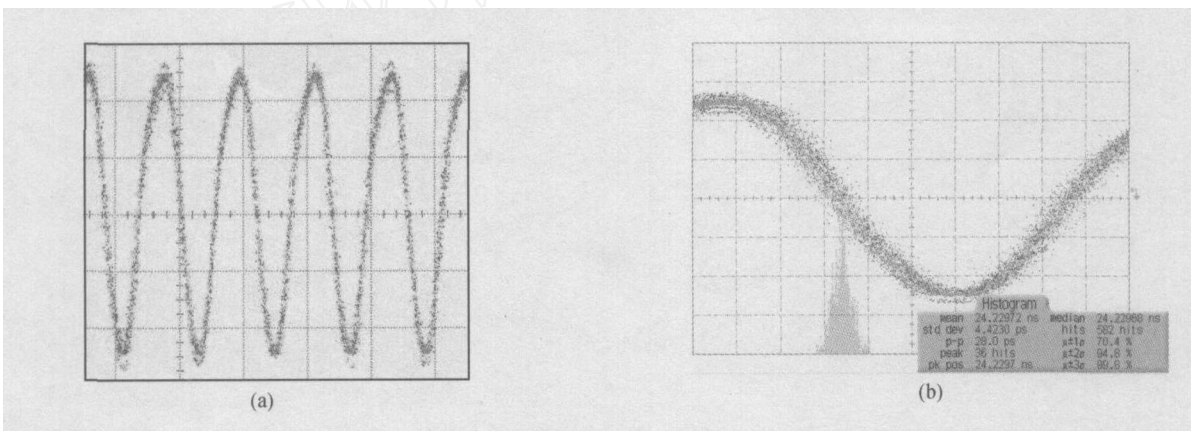

Fig. 15　(a) Measured PLL output waveform (200ps/ div) in time domain at 4. 22GHz ; (b) Jitter of the output

6　Conclusion

A monolithic LC-VCO with two tuning terminals was realized using 0. 18μm CMOS technology. It exhibits a phase noise of - 107dBc/ Hz at 500kHz off the center frequency. The frequency of the output signal can cover 4. 1～4. 3GHz, the range of the transceivers for WLAN. The topology with two tuning terminals can improve the performance of the circuit. The IC can be used in a WLAN transceiver.

References

[1] IEEE Standard 802. 11a. Wireless LAN medium access control (MAC) and physical layer (PHY) specification, 1999

[2] Razavi B. Design considerations for direct-conversion receivers. IEEE Trans Circuits Syst Ⅱ: Analog and Digital Signal Processing, 1997, 44(6) :428

[3] Behzad A R, Zhong M S, Anand S B, et al. A 5-GHz direct-conversion CMOS transceiver utilizing automatic frequency control for the IEEE 802. 11a wireless LAN standard. IEEE J Solid-State Circuits, 2003, 38(12) :2209

[4] Dulger F, Sanchez-Sinencio E. Design trade-offs of a symmetric linearized CMOS LC VCO. IEEE International Symposium on Circuits and Systems, 2002, 4 :26

[5] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2) :179

[6] Huang Ting. Research of key technologies for ultra-high-speed, radio frequency and microwave monolithically integrated circuits design. PhD Dissertation, Southeast University, 2004(in Chinese)

[7] Kinget P. A fully integrated 2. 7V 0. 35μm CMOS VCO for 5GHz wireless applications. Digest of Technical Papers of IEEE International Solid-State Circuits Conference, 1998

[8] Yang Fenglin, Zhang Zhaofeng, Li Baoqi, et al. A 4. 8GHz CMOS fully integrated LC balanced oscillator with symmetrical noise filter technique and large tuning range. Chinese Journal of Semiconductors, 2005, 26(3) :448

4 GHz 级频率综合器下单片低相位噪声 CMOS 电感电容压控振荡器的设计 *

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摘要: 基于 0.18μm RF CMOS 工艺,采用双端调谐结构实现了一种可应用于 WLAN 的二次变频收发机的压控振荡器. 其输出频率范围可以覆盖收发机所需 4.1～4.3GHz 的频段,其最大调谐范围为 500MHz. 在距中心频率 4.189GHz 为 4MHz 处的相位噪声为 - 117dBc/ Hz,500kHz 处为 - 107dBc/ Hz. 输出信号抖动的均方根值为 4.423ps,输出功率为 - 8.68dBm.

关键词: 压控振荡器; PLL; WLAN; 收发机

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