An Implementation of a CMOS Down-Conversion Mixer for GSM1900 Receivers

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Abstract: A 1.9GHz down-conversion CMOS mixer with a novel folded Gilbert cell, intended for use in GSM1900 (PCS1900) low-IF receivers, is fabricated in a RF 0.18μm CMOS process. The prototype demonstrates good performance at an intermediate frequency of 100kHz. It achieves a conversion gain of 6dB, SSB noise figure of 18.5dB (1MHz IF), and IIP_3 11.5dBm while consuming a 7mA current from a 3.3V power supply.

Key words: GSM receiver; low-IF; mixer; CMOS RF integrated circuits
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1 Introduction

Current interest and demand for portable wireless communication services have increased the emphasis on the development of low-power, low-cost radio-frequency communication integrated circuits (RFIC). Mixer is one of the most important modules for RF transceivers. This paper presents the design and implementation of a CMOS high frequency down-conversion mixer, shown in Fig. 1, suitable for a single-chip receiver. The receiver topology proposed here is designed to meet the personal communications standard (PCS1900). A low-IF architecture is adopted in the receiver for PCS's relaxed adjacent channel rejection. This architecture can also lower the power of $1/f$ noise by 4.7dB[1].

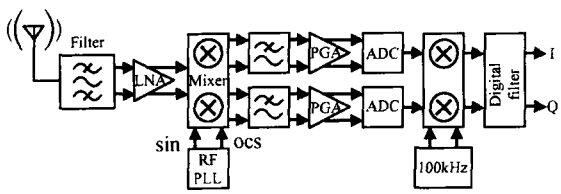

Fig. 1 GSM1900 low-IF receiver architecture

Several mixer topologies were recently reported in Refs. [2,3]. The mixer proposed in Ref. [2] employs a source-follow trans-conductance stage to improve linearity performance; however, it produces no gain. Reference [3] employs a traditional Gilbert cell structure, but it demonstrates poor linearity performance. The mixer proposed here is based on a novel folded Gilbert cell topology, which is shown in Fig. 3. This mixer topology is similar to the classical Gilbert cell based mixer (Fig. 2). Both mixers use a balanced trans-conductance stage and four switching transistors. One of the main advantages of the proposed topology is its use of tank

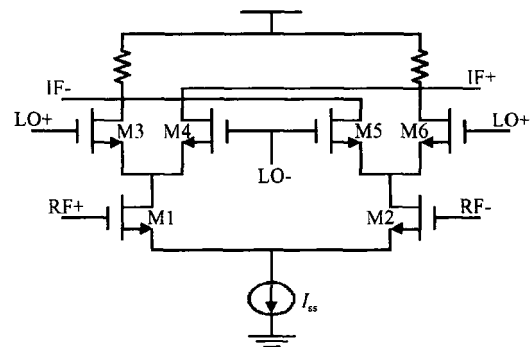

Fig. 2 Topology of the traditional Gilbert cell of a mixer

circuits to fold the RF signal to the switching pairs, thus retaining the same advantages as the Gilbert cell based mixer. With this folded topology, we can set the bias current of the trans-conductance stage and the commutate stage independently, and the noise and linearity performances can then be optimized independently. In addition, the folded structure and the LC tank used here make

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this topology suitable for low-voltage circuit design, and the pMOSFET commutate stage generates less 1/ f noise, which sometimes dominates the noise performance of mixers in low-IF systems[4].

2 Design of the mixer

2.1 Principles and design considerations

A schematic of the proposed mixer is shown in Figs. 3 and 4. It includes a mixer core, an LO buffer, and bias circuits. For the mixer core design, M3 ~M6 pMOS cross-coupling cells are used for the mixer current commutation stage and M1, M2 nMOS pairs for the trans-conductance stage. The RF input signal is injected through the nMOS pair into nodes X and Y, and the pMOS commutation pairs modulate the input signal according to the sinusoidal LO signal to produce a down-converted IF output signal through two off-chip resistor loads, facilitating circuit testing. Two inductors, L_{d1} and L_{d2}, co-operate with C_1 and C_2 (including the parasitic capacitances) at points X and Y, which ensure resonance at the central frequency of the input signal. The LC tank is used in the circuit design for narrow-band, low voltage, and low power purposes[5]. L_{s1} and L_{s2} are two inductors used as inductive degenerators that are similarly used in the LNA input stage. These inductors are good for both the conjugate matching of the mixer input and good linearity performance[5]. The capacitance C_c is used to prevent an LO signal and its harmonic products from the LO port feedthrough to the RF/ IF ports. Therefore, it helps not only the isolation between the LO and IF ports, but also the circuit performance after the mixer.

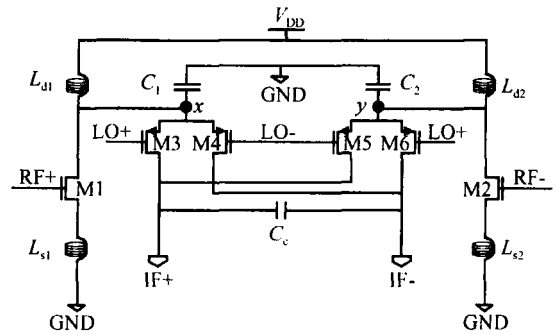

Fig. 3 Proposed mixer core circuit with folded topology

A differential-in, differential-out common source amplifier topology LO buffer is employed in the design, as shown in Fig. 4. Mb1 and Mb2 compose the major amplifier stage. The source current I_{bias1}, together with Mb3 and Mb4, provides the current bias. R_L and C_L, configured as a low pass filter, are used to suppress high frequency noise from the bias circuits.

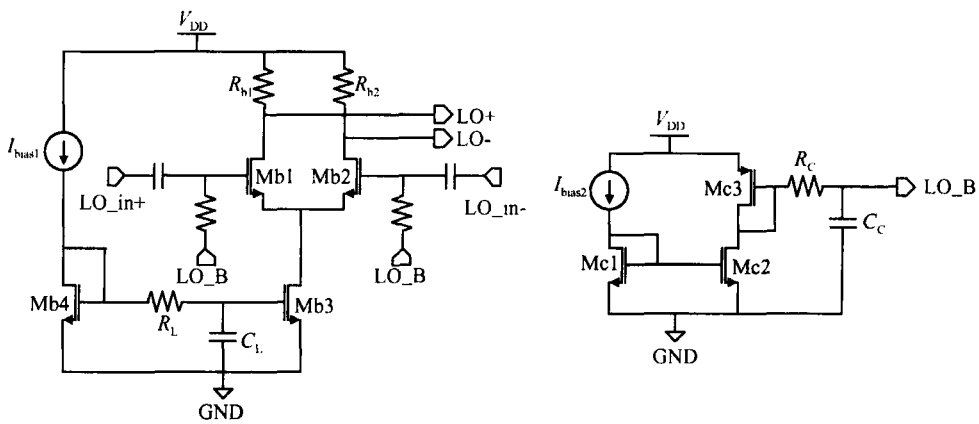

Fig. 4 LO buffer and bias circuits

The sizes of Mb1, Mb2, R_{b1}, and R_{b2} should be optimized for a large output signal swing. The LO signal should be large enough to ensure that the zero crossing slope of the sinusoidal LO signal is sharp enough to achieve the best noise and linearity performance. In particular, the LO buffer should be designed with high linearity and good noise performance to minimize its noise and nonlinearity

contributions to the core circuit. The bias circuits for both the LO buffer and mixer core are also shown in Fig. 4.

2.2 Noise and linearity analysis

2.2.1 Noise analysis

Mixers are significant noise contributors in most communication systems because they can mask a weak desired signal, and mixing functions are inherently noisy. However, it is difficult to calculate the noise profile of a mixer due to the cyclostationary nature of the noise sources. For a low IF mixer, the dominant noise contribution comes from low frequency noise (nearly 90 % according to our simulations), so we focus our flicker noise analysis here.

The low frequency noise, including flicker noise, is up-converted to ω_0 and its harmonics in the trans-conductance stage. This means the trans-conductance MOSFETs only contribute white noise after frequency translation since the $1/f$ corner is usually far beyond the LO frequency. A small amount of flicker noise in the trans-conductance MOSFETs appears at the loads due to the mismatch in the switching pairs. However, the flicker noise in the switching pairs is a major concern for a mixer in zero-IF and low-IF systems. Sometimes it even dominates the noise performance of a mixer if the IF frequency is around or below the $1/f$ noise corner. The flicker noise can be referred as a voltage source at the gate of the switching transistors with a constant RMS value V_n[4],

$$V_n^2 = 2 \times \frac{K_f}{W_{eff} L_{eff} C_{ox} f} \tag{1}$$

where K_f and C_{ox} are the technology constants. This voltage is just like a slowly varying offset voltage associated with switching pairs. This offset voltage advances or retards the time of zero-crossing $\Delta t = V_n(t)/S$, where S is the slope of the LO voltage at the switching time[7,8]. The output flicker noise can be modeled simply as

$$i_{o,n}(f) = \frac{4I}{ST} \times V_n(f) = \frac{1}{\pi} \times \frac{I_{ss}}{A} \times V_n(f) \tag{2}$$

where I_{ss} is the total bias current of the switching pairs, S is the zero-crossing slope of the LO, and T and A are the period and the amplitude of the LO signal. It is known that mixers suffer a large flicker noise with a high bias current in the switching pairs. Thus, in order to get a small noise figure, the current of the commutation stage in this folded mixer can be set relatively small; however, this cannot be realized in a traditional Gilbert mixer.

2.2.2 Linearity analysis

The linearity performance requirement is critical in modern RF communication systems. Especially for cell phone applications, a highly linear receiver is required for immunity to various interference signals. The linearity of the mixer is more important since the input signal of the mixer is an amplified signal from the LNA, and it significantly affects the dynamic range (DR) of the receiver. The linearity performance of the CMOS trans-conductance stage is of major concern in the design of a mixer[5]. The most effective way to improve the non-linearity effects is to add a negative feedback in the circuit. An inductance feedback is used in the mixer design. This is because the inductive degeneration introduces less thermal noise while consuming almost no DC headroom. Second, the inductive impedance increases with the frequency, increasing the AC feedback and restraining high frequency harmonics. Third, it is also beneficial for input impendence matching as is often done in the input impedance matching of an LNA.

Many methods for analyzing the linearity of a mixer were proposed in Refs. [10, 11]. Figure 5 shows the spice-model of the trans-conductance MOSFET. Z_g is the impendence at the gate of the input transistor, which includes the bias shunt resistance. Z_s is the impendence at the transistor source, including the parasitic source resistor r_s. The dominant non-linearity components of the input trans-conductance stage are g_m, C_{gs}, and C_{gd}. The C_{gd} effect should not be neglected, although it

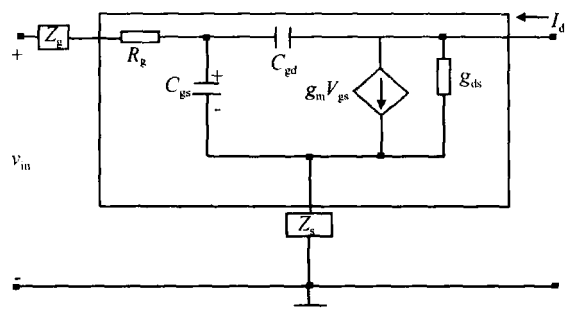

Fig. 5 Nonlinearity model of the trans-conductance MOSFET

is relatively small compared to C_{gs} in the saturate region. C_{gd} is equivalent to a capacitance parallel to C_{gs} according to Miller effects. Here a simplified IIP_3 of the Gilbert cell mixer used in many reports[11,12] is employed. The linearity of the proposed mixer has the same characteristics as a Gilbert cell mixer when neglecting the non-linearity effects of the switching pairs and the load of the trans-conductance stage.

The small signal I-V relationship can be expressed in a Taylor series, which is usually used for weakly nonlinear behavior analysis:

$$I_o = f^{-1}(V_{in}) = c_1 V_{in} + c_2 V_{in} + c_3 V_{in} + \cdots \quad (3)$$

$$IIP_3 = dB_{20}\sqrt{\frac{4c_1}{3c_3}} = dB_{20}\sqrt{\frac{16I_{ss}}{3k}} \quad (4)$$

Here I_{ss} is the total state current of the trans-conductance pair, and k is the parameter of M1 and M2 in Fig. 2. It can be seen that the linearity performance can be improved by increasing the bias current of the trans-conductance transistors. More detailed analysis of the linearity can be found in Refs. [6, 13].

2.3 Design trade-off and optimization

According to the above analysis, there are many design trade-offs among power, linearity, gain, and noise. In a traditional Gilbert cell mixer, the linearity performance is determined by the trans-conductance stage, and the noise performance is often dominated by the switching pairs, especially for a mixer in low-IF receivers. As described in Eq. (4), a higher bias current in the trans-conductance stage I_{ss} is required to achieve better linearity performance. From Eq. (2) however, a higher switching bias current induces a higher noise output due to the switching pairs while simultaneously producing a higher switching pair nonlinearity. Consequently, the linearity and noise performance conflict in the design of a Gilbert cell based mixer. The folded structure (Fig. 3) proposed in this paper, however, overcomes this design conflict. The bias current of the trans-conductance stage and the switching stage can be set independently: the bias current of the trans-conductance stage can be set large enough to meet the requirement of gain and linearity, while the bias current of the switching stage can be set relatively small to reduce the flicker noise and non-linearity in the switching pair.

3 Implementation and measurements

The GSM1900 Receiver was fabricated with SMIC 0.18μm CMOS RF technology. The die micrograph of the mixer is shown in Fig. 6. The active area of the mixer with LO buffer is 0.8mm × 0.7mm. The testing instruments include a spectrum analyzer E4440A, vector network analyzer E5071B, RF signal generator E4438C, and noise source E346C from Agilent Technologies™. The measured performance of the mixer is summarized in Table 1. Figure 7 shows the measured output spectrum of the mixer. Considering the losses of the microwave connector and the single to differential balun, the conversion gain of the mixer at 100kHz IF is about 6dB. In order to evaluate the linearity of the mixer, a two-tone inter-modulation measurement was carried out with tone frequencies at 1900 and 1900.2MHz. Figure 8 shows the IIP_3 results. Due to equipment limitations, the SSB noise figure of the mixer could only be measured to be 18.5dB at a 1MHz (instead of 100kHz) IF output.

Table 1 Measured mixer performance

Mixer	Parameter
Supply voltage	3.3V
Current dissipation	7mA
RF frequency	1900MHz
LO frequency (4dBm)	1900.1MHz
SSB (noise figure)	18.5dB
Power conversion gain	6dB
Input IP_3	11.5dBm
Input 1dB compression level	1.5dBm
LO-RF feed-through	- 53dB
LO-IF feed-through	- 48dB

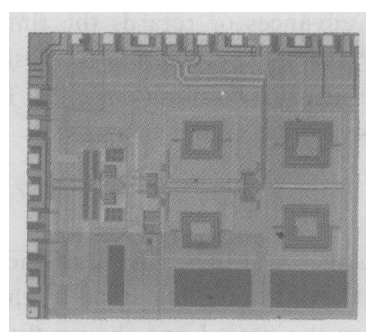

Fig. 6 Micrograph of the mixer die

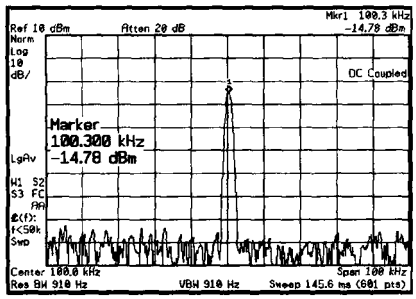

Fig. 7 Measured mixer output spectrum RF input power is - 20dBm/1900MHz and LO power is 4dBm/1900.1MHz.

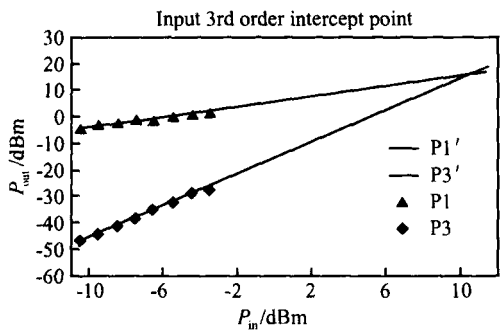

Fig. 8 Extrapolation of the mixer IP_3

4 Conclusion

A 1.9GHz down-conversion CMOS mixer with the utilization of a novel folded Gilbert cell fabricated in a RF 0.18μm CMOS process has been described. The mixer module, including a mixer core and LO buffer, achieves good performance. The measurements show that the performance of this mixer meets the requirements of the low-IF GSM1900 receiver system.

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一种新型的基于 GSM1900 标准的 1.9GHz CMOS 混频器

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摘要: 介绍了一种 0.18μm CMOS 工艺基于 GSM1900(PCS1900)标准低中频接收机中的混频器. 该混频器采用了一种新型的折叠式吉尔伯特单元结构. 在 3.3V 电源电压、中频频率为 100kHz 的情况下, 该混频器达到了 6dB 的转换增益, 18.5dB 的噪声系数(1MHz 中频)和 11.5dBm IIP_3 的高线性度, 同时仅消耗 7mA 电流.

关键词: GSM 接收机; 低中频; 混频器; CMOS 射频集成电路
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