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Room Temperature Resonant Tunneling and Negative Differential Resistance Effects in a Self-Assembed Si Quantum Dot Array*

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Abstract: We report the room temperature resonant tunneling and negative differential resistance (NDR) effects in a self-assembled Si quantum dot (Si-QDs) array. The double-layer structure of Al/SiO_2/Si-QDs/SiO_2/p-Si substrate is fabricated by layer-by-layer deposition and *in situ* plasma oxidation in a plasma-enhanced chemical vapor deposition (PECVD) system. Obvious NDR effects are directly observed in the current-voltage characteristics, and similar peak structures at the same voltage are also identified in the capacitance-voltage characteristics. Both of them are attributed to the resonant tunneling and charging dynamics in the Si-QD array. Moreover, the major features, such as the scan-rate and scan-direction dependences of the peak structure, are investigated, and the underlying mechanism is found to be quite different from that of a quantum well structure. Based on a master-equation numerical model, the resonant tunneling and charging dynamics together with the unique features can be satisfactorily explained and reproduced.

Key words: Si quantum dot array; NDR; resonant tunneling
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1　Introduction

The resonant tunneling and NDR effects in double barrier structures have been the focus of much research in recent decades[1~4] due to both interest in the fundamental physics and potential applications in the design of high speed logic devices[5,6]. More recently, resonant tunneling through the discrete levels in QDs has become a new focus in the study of electronic transport properties because of the novel quantum confinement and Coulomb blockade effects in nanometer-scaled structures[7,8]. However, there is still great difficulty in the precise fabrication and direct control of single QDs in device applications[8]. Thus, it is particularly important to study the resonant tunneling and NDR effects in QD arrays, in order to utilize their unique transport properties in future device design. Among the many approaches employed to fabricate ultra-small QDs in different materials for applications in devices, self-assembled Si-QDs are considered one of the most promising candidates for future applications, which could be exploited for their inexpensive mass production of well-defined high density QDs with good size dispersion.

In this paper, we demonstrate the room temperature resonant tunneling and NDR effects in a self-assembled Si-QD array, in which the density is about $5 \times 10^{11}\ cm^{-2}$ with an individual spherical QD size of 6nm and a deviation of less than 10%, which provides a good basis for the observation of collective resonant tunneling and NDR effects in the a Si-QD array. We further compare the resonant tunneling and NDR effects of a Si-QD array to those of a quantum well (QW) structure and then discuss their different underlying mechanisms. A master-equation-based numerical model is established, and the observed scan-rate and scan-direction dependences, which are related to the tunneling and charging dynamics in the Si-QD array, are well explained and reproduced. Thus, we provide direct experimental evidence for the resonant tunneling and NDR effects in a Si-QD array, which has important application potential

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in future quantum logic devices.

2 Sample fabrication and measurement

The Al/SiO_2/Si-QDs/SiO_2/p-Si structure was fabricated on substrates of p-type (7～9Ω・cm) crystalline silicon (100) in a plasma-enhanced chemical vapor deposition (PECVD) system at 250℃. First, a tunneling SiO_2 layer of 2nm was formed by plasma oxidation directly on the silicon substrate. Then, a Si-QD array layer was fabricated from a hydrogen-diluted silane gas mixture with a layer-by-layer deposition technique. Finally, a thinner gate SiO_2 layer was made *in situ* by plasma oxidation again under similar conditions as those of the tunneling SiO_2 layer. The details of the sample fabrication were reported in our previous work[9]. After that, the samples were annealed in N_2 ambient at 900℃ for 30min, which is essential to the final formation of the well-defined Si-QDs[10] and to the reduction of interface states and defects in the structure. Al electrodes with an area of $0.8\times10^{-3}cm^2$ on the topside and backside were made with the vacuum evaporation method.

Atomic force microscopy (AFM) was used to characterize the size and the distribution of the Si-QD array in the sample. Figure 1 is a plane-view AFM image of the Si-QD array after the gate SiO_2 layer was removed with a diluted HF solution. As

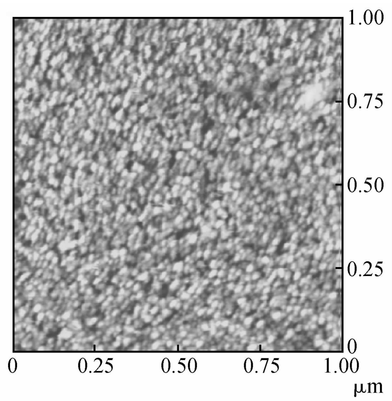

Fig.1 A plane-view AFM image of the Si-QD array after the gate SiO_2 layer is removed with diluted HF solution

shown in the image, the shape of the Si-QDs is roughly spherical, and the mean diameter is 6nm, with a deviation of less than 10%. The density of the Si-QDs is estimated to be $5\times10^{11}cm^{-2}$. A cross section image obtained by transmission electron microscopy (TEM) of the sandwiched structure is shown in Fig.2, where the interfaces between the different layers are clear and abrupt.

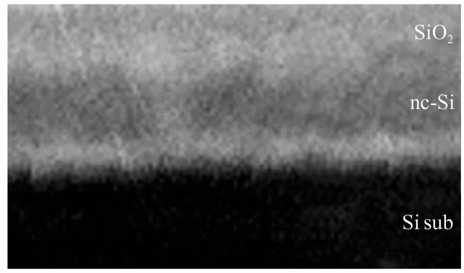

Fig.2 Cross-section TEM photograph for the as deposited structure

The *I-V* characteristics were measured using an HP4156C precision semiconductor parameter analyzer, while the *C-V* characteristics were measured using an HP4294A precision impedance analyzer, at room temperature.

3 Results and discussion

The typical current-voltage characteristics are shown in Fig.3(a). (For convenience, the coordinate system is rotated to make the *x*-axis and *y*-axis range from 0 to negative values.) As indicated in Fig.3(a), an obvious NDR effect region can be identified in the voltage range of about −1.8～−2.2V. There are two remarkable features: (1) in the forward (0～−3V) sweep, with the increase of the scan-rate, the falling edge of the first peak shifts forward to become more negative, and the peak height "rushes" to higher current values; the second peak, however, is totally independent of the scan-rate; (2) In the backward (−3～0V) sweep, the reverse sweep shows a suppressed-peak structure and the positions of the peak shift backward. These features are apparently different from the previously reported NDR effects observed in quantum well structures[1～3]. As will be discussed later, these features are related to the unique tunneling and charging effects of Si-QD arrays.

In the *C-V* characteristics, we observe a similar peak structure with the same peak position as that in the *I-V* characteristics. Moreover, the relative heights of the first and second peaks are also

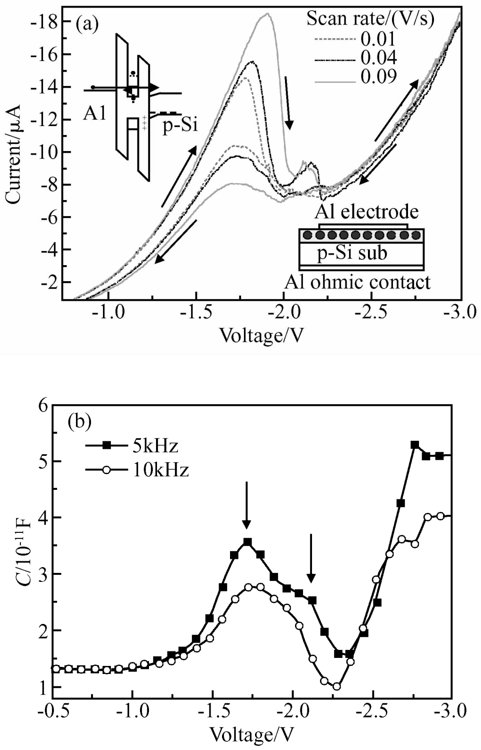

Fig. 3 (a) A typical *I-V* curve with obvious NDR peaks for different scan rates The forward and backward traces are indicated by arrows. The schematic band diagram under negative bias and a sample structure are shown in the top left and bottom right insets, respectively; (b) A typical frequency-dependent capacitance-voltage (*C-V*) characteristic

consistent with those in the *I-V* characteristics. According to our previous study, the frequency-dependent capacitance peak structure originates from the resonant tunneling response of the discrete confinement levels in Si-QDs[9], which gives direct information about the levels' positions in Si-QDs and their relative density of states. Together with the *I-V* characteristics, the *C-V* characteristics provide direct evidence that the peak structure and NDR are related to the resonant tunneling through the Si-QD array.

Further analysis reveals that the major contribution to the tunneling current is electron injection from the Al electrode rather than hole injection from the p-Si substrate. As shown in the energy diagram in the top left inset of Fig. 3(a), under negative bias (0～−2.7V), the holes in the substrate are still expelled from the substrate interface due to the residual fixed positive charged in the barrier layer (which causes a positive surface potential in substrate), which is directly proven by the flat-band voltage position (−2.7V) in the *C-V* measurements.

The difference between the underlying mechanisms for the resonant tunneling and NDR effects in the Si-QD array and the QW structure lies in two facts: (1) The resonant tunneling through the Si-QD array, where each individual QD contributes one "resonant tunneling path", is directly affected by the number of QDs N_{QDs} that provide tunneling levels. (2) Due to the ultra-small size effects of the QDs (just a few nm), the Coulomb blockade energy E_{CB}, resulting from the charging or trapping of one electron in the dot region, can be large enough to shift the resonant level out of the resonant tunneling voltage region and eventually pinch the "tunneling path" through this dot.

In our case, the size of the spherical Si-QDs is about 6nm, and the Coulomb blockade energy is simply estimated according to a semi-classical constant interaction (CI) model (without consideration of the image forces):

$$E_{CB} = q^2/C_{QDs} = 120\text{meV} \quad (1)$$

Here $C_{QDs} = 4\pi\varepsilon_0\varepsilon_{SiO_2}R = 1.5\text{aF}$, where R is the radius of the dots and q is the elementary charge. Meanwhile, the quantum confinement energy level for the dot is estimated in an infinite spherical square well model to be $E_{n,l} = \dfrac{\hbar^2}{2m_{Si}R_{QDs}^2} \times \chi_{n,l}^2$, where $\chi_{n,L}$ is the nth zero-point of the spherical Bessel function $j_l(r)$, and the effective mass of the electron in silicon is $0.26m_0$, where m_0 is the electron rest mass. The ground state energy is about $E_{QC}^{1,0} = E_{1,0} \approx 160\text{meV}$, and the interval between the ground state and the first excited state is about $E_{QC}^{2,1} = E_{2,0} - E_{1,0} \approx 160\text{meV}$, which in our case is close to the Coulomb charging energy E_{CB}.

The level-arm-factor for the layered structure is directly estimated to be

$$\alpha = d_g/(d_g + d_d + d_t) \approx 0.2 \quad (2)$$

where d_g, d_d, and d_t are the thicknesses of the gate, Si-QD array, and tunneling layers, respectively. Therefore, the voltage position of the major resonant energy level can be estimated to be

$$V = (E_{QC} + E_{CB}/2 + W_{Al\text{-}pSi})/q\alpha \approx -2.1\text{V} \quad (3)$$

where $W_{Al\text{-}SiCB}$ is the energy difference between the Fermi level of Al and the conduction band edge of Si. This agrees well with the observed second peak's position. Moreover, we estimate the voltage shift of the energy level in a QD when it is charged with one electron to be

$$V_{\text{shift}} = E_{\text{CB}}/q\alpha = -0.6\text{V} \quad (4)$$

which is large enough to shift the level (by -0.6V) out of the resonant region. Based on the above analysis, we can conclude that the peak structure observed in both the *I-V* ad *C-V* characteristics can be attributed to the resonant tunneling through the single confinement level in the QDs, and the Coulomb blockade energy can readily pinch the resonant tunneling path when it is charged with one electron.

As shown in the *I-V* characteristics, the resonant tunneling current (superimposed on a background current) increases as the emitter Al Fermi level approaches the discrete confinement levels in the Si-QD array. However, there is also a chance that the electrons will be charged (trapped) into the QDs and relaxed into the QDs' related defects or interface states, which are more stable and localized[11]. As we mentioned above, once every QD in the array is charged with one electron, the resonant tunneling current through the confinement energy levels is pinched abruptly, giving rise to an obvious NDR effect region. The scan-rate dependence is due to the fact that a fast scan takes more time (in the bias range) to charge a fixed number of QDs N_{QDs}. As to the second peak observed in both the *I-V* and the *C-V* characteristics, we attribute it to the bi-stable transport properties near the valley of the NDR region. In the reverse sweep from high negative bias, the resonant tunneling current is greatly suppressed until the discharging (detrapping) of electrons from the Si-QD array.

Moreover, in order to further study the tunneling and charging dynamics that occur in the Si-QD array, a master-equation-based numerical simulation model is established. The key parameters involved in the model are the number of QDs $N_{\text{QDs}} = S_{\text{electrode}} D_{\text{QDs}}$ (estimated from the electrode area and the density of the Si-QD array), the charging (trap) and discharging (detrap) rates of σ_{trap} and σ_{detrap}, the Coulomb charging energy E_{CB}, the quantum confinement energy E_{QC}, and the temperature kT_{B}. The definition of the resonant tunneling current is proportional to the number of QDs that contribute a resonant level to the tunneling:

$$I \propto \int D_{\text{electrode}}(E) f(E) T(E) N_{\text{dots}}(E) \mathrm{d}E \quad (5)$$

Here the transmission coefficient is assumed to take on a Lorentzian form:

$$T \propto (1 + (E - E_{\text{level}})^2 / kT_{\text{B}}^2)^{-1} \quad (6)$$

This is characteristic for a continuum electron state incident on the resonant levels in a Si-QD array. As shown in Fig. 4(a), the forward sweep with different scan rates is demonstrated, and the major features are well-captured, including the shift of the first peak and the relative peak heights. In Fig. 4(b), the different peak structures together with their evolution with the scan rate can be satisfactorily explained and reproduced. Good agreement between the experimental and simulation results helps to further understand the details of the unique tunneling and charging dynamics in the Si-QD array, and to explain the distinct mechanism compared with that of quantum well structures. However, further study is needed to reveal the detailed mechanism that governs the tunneling and charging dynamics of Si-QD array systems.

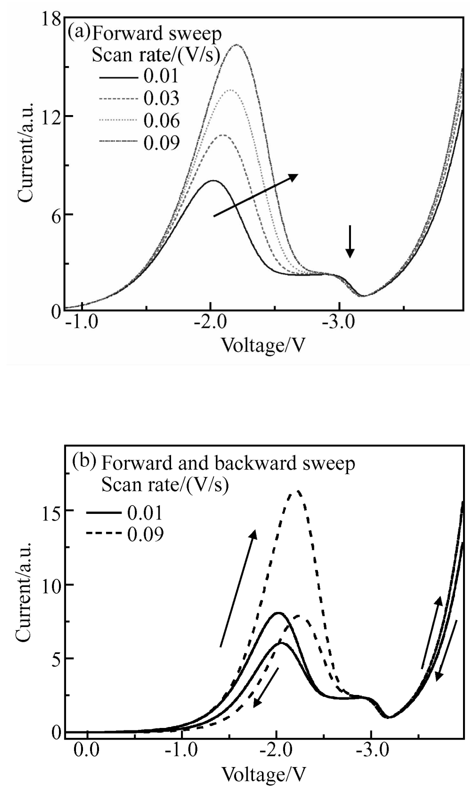

Fig.4 Numerical simulation results for the *I-V* characteristics of the resonant tunneling and charging dynamics of the Si-QD array (a) For the forward sweep with different scan rates; (b) For the forward and backward sweep at two different scan rates

4 Conclusion

In summary, we have reported the room temperature resonant tunneling and NDR effects in a self-assembled Si-QD array, in which the unique tunneling and charging dynamics, manifesting themselves both in the *I-V* and *C-V* characteristics, originate from the quantum confinement and Coulomb blockade effects of the Si-QD array. A numerical model is established to illustrate the details of the underlying mechanism, which is different from that of a quantum well structure. Thus the experimental and theoretical basis for the application of a self-assembled Si-QD array in future electronic logic devices has been laid.

References

[1] Chang L L, Esaki L, Tsu R. Resonant tunneling in semiconductor double barriers. Appl Phys Lett, 1974, 24 (12): 593

[2] Morris D P, Price P J. Resonant tunneling through a diode accumulation layer. J Appl Phys, 1999, 85(5): 2694

[3] Buot F A, Zhao P, Cui H L. Emitter quantization and double hysterisis in resonant-tunneling structures: a nonlinear model of charge oscillation and current bistability. Phys Rev B, 2000, 61(8): 5644

[4] Qiu Z J, Gui Y S, Guo S L, et al. Experimental verification on the origin of plateau-like current-voltage characteristics of resonant tunneling diodes. Appl Phys Lett, 2004, 84(11): 1961

[5] Chow D H, Dunlap H L, Williamson W, et al. An efficient HBT/RTD oscillator for wireless applications. IEEE Electron Device Lett, 1996, EDL-17(2): 69

[6] Inokawa H, Fujiwara A, Takahashi Y. Multi-peak negative-differential-resistance device by combining single-electron and metal-oxide-semiconductor transistors. Appl Phys Lett, 2001, 79(22): 3618

[7] Kastner M A. The single electron transistor. Review of Modern Physics, 1992, 64(3): 849

[8] Bukowski T J, Simmons J H. Quantum dot research: current state and future prospects. Critical Review in Solid State and Materials Sciences, 2002, 27(3): 119

[9] Shi Jianjun, Wu Liangcai, Huang Xinfan, et al. Electron and hole charging effect of nanocrystalline silicon in double-oxide barrier structure. Solid State Commun, 2002, 123(1): 437

[10] Zhang Lin, Chen Kunji, Wang Liangcai, et al. The dependence of the interface and shape on the constrained growth of nc-Si in a-SiN_x/a-Si : H/a-SiN_x structures. J Phys: Conden Matter, 2002, 14(2): 10083

[11] Kirton M J, Uren M J. Capture and emission kinetics of individual Si : SiO_2 interface states. Appl Phys Lett, 1986, 48 (19): 1270

自组装 Si 量子点阵中室温共振隧穿及微分负阻特性*

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摘要: 报道了自组装 Si 量子点(Si-QDs)阵列在室温下的共振隧穿及其微分负阻特性.在等离子增强化学气相沉淀系统中,采用 layer-by-layer 的淀积技术和原位等离子体氧化方法制备了 Al/SiO_2/Si-QDs/SiO_2/Substrate 双势垒结构.通过原子力显微镜和透射电子显微镜检测,证实所获得的 Si-QDs 阵列中 Si 量子点平均尺寸为 6nm,并具有较好的尺寸均匀性(小于 10%).在对样品的室温 *I-V* 和 *C-V* 特性的测量中,直接观测到由于 Si 量子点中分立能级而引起的共振隧穿和充电效应:*I-V* 特性表现出显著的"微分负阻特性(NDR)";而 *C-V* 特性中也同样观测到位置相对应、结构相似的峰结构,从而证实了 *I-V* 和 *C-V* 特性中的峰结构都同样来源于电子与 Si 量子点阵列中分离能级之间的共振隧穿和充电过程.进一步研究发现,Si 量子点阵列中共振隧穿和 NDR 特性所特有"扫描方向"和"速率"依赖性及其机制,与量子阱的情况有所不同.通过所建立的主方程数值模型,成功地解释并重复了 Si 量子点阵中共振隧穿所特有的输运特性.

关键词: Si 量子点阵列; NDR; 共振隧穿

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