Design of a Low Noise, Low Power Audio Power Amplifier for Driving Headphones

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Abstract: This paper describes the design and implementation of a low noise, low power, programmable-gain audio power amplifier used as a headphone driver. It obtains a 0.1% THD + N with a 5V power-supply, a 1kHz frequency audio signal, and a 120mW continuous average output power into a 16Ω load. In addition, the gain can be set from +12 to −34.5dB in 32 discrete steps of 1.5dB. The amplifier is used as the core of a programmable gain audio power amplifier for driving headphones. The audio power architecture, the main module circuits of the amplifier design, the test results, and the chip layout are included. Experimental results using a CSMC 0.6μm double poly double metal CMOS process show that the required performance can be obtained.

Key words: audio power amplifier; low noise; low power
EEACC: 1220; 1280
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2006)S0-0029-03

1 Introduction

Currently, portable electronic devices such as cellular phones, MP3 players, CD players, DVD players, and PDAs are widely used, increasing the need for an audio power amplifier that drives headphones to create sound. A programmable gain amplifier is realized in this paper. Its voltage gain range is from +12 to −34.5dB by 1.5dB steps. It must also have low power consumption and be able to run with a 5V power supply. According to the AC97 Specification Rev. 2.3[1], it must have very low noise.

This paper describes a programmable-gain, differential-difference amplifier for an audio power amplifier chip. It begins by discussing the architecture of the audio power amplifier. Then a number of key circuits used in the amplifier are described. Finally, some results and conclusion are presented.

2 Audio power amplifier architecture

A differential-difference amplifier solution[2] presents high input impedance and weak linearity performance. The realization uses bipolar devices but is not applicable to a system on a chip (SOC). We have chosen a full CMOS approach for the audio power amplifier and a differential resistor string with logarithmically spaced taps for voltage-gain programming.

The audio power amplifier mainly includes an amplifier, a bias voltage generator, a digital gain control, and other circuits, as shown in Fig. 1. The amplifier is composed of an input differential stage, a middle stage, and an output stage.

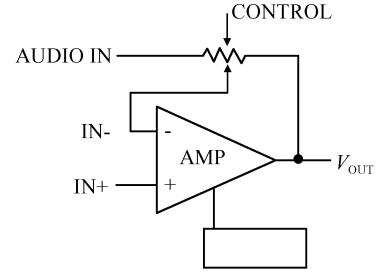

Fig. 1 Architecture of the audio power amplifier

3 Amplifier

The core of the amplifier circuit is composed of 3 main blocks: a differential input stage, an output stage, and a frequency compensation stage. The low noise requirements, 1μVrms in the band 100Hz~44kHz, dictate rather low input and feedback resistors. A low impedance output stage en-

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Received 11 October 2005, revised manuscript received 28 December 2005

sures constant accuracy and speed for load changes with programmed gain.

3.1 Differential input stage

A schematic of the differential input stage is shown in Fig. 2. A pMOS input pair is preferred for its lower $1/f$ noise[3]. $\overline{i_n^2} = \frac{K}{f} \times \frac{g_m^2}{WLC_{ox}^2} \times \Delta f$, where K is the coefficient of the MOSFET, and the K of the pMOS typically equals $10^{-28} C^2/m^2$, which is much smaller than that of nMOS. At the same time, the thermal noise of pMOS is also less than that of nMOS.

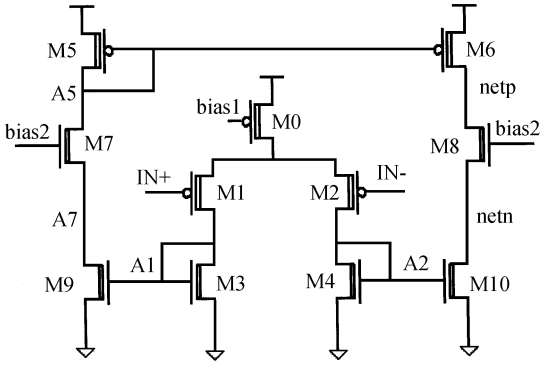

Fig. 2 Amplifier differential input stage

The load is active in order to realize a high gain voltage with only two stages. In this way, the frequency compensation is simplified. Therefore, we did noise optimization only on this first stage because the noise voltage of the following stages is divided by the first stage voltage gain[4]. Following the guidelines for a low $1/f$ noise, two steps are taken: (1) high aspect ratio for input devices; (2) long channel active loads. The important fact here is that for the active loads M3 and M4, which are static devices, there is no tradeoff between the low $1/f$ noise requirements and speed. Therefore M3 and M4 are very long channel devices. The W/L ratio is kept reasonable in order to ensure a good saturation margin.

In order to get a high gain, the second gain stage is built with a cascode structure biased at a constant 50μA. The noise contribution from the biasing stages appears in the common mode on nodes A1 and A2, and it is cancelled by the differential topology. If perfect symmetry is respected in the layout of the four devices M1～M4, cancellation is effective. In this case, optimum noise performance can be predicted by simulation and can be reached.

3.2 Output stage

The output stage has to deliver power to the load (headphone) in response to the input signal. In other words, it has to realize a power gain that usually consists in a current gain. The audio output stages general require low harmonic distortion, high voltage dynamics, low output resistance, driving capability of high reactance loads, high reliability, and protection against overloads and short-circuits[5]. The output stage of the amplifier is represented in Fig. 3. A class AB output stage is selected[6], in which M12 and M13 are common-source.

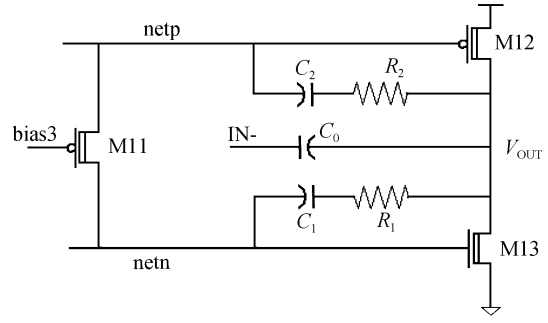

Fig. 3 Amplifier output stage and frequency compensation

3.3 Frequency compensation

The amplifier frequency compensation is shown in Fig. 3. In order to obtain frequency compensation, compensation networks R_1, C_1 and R_2, C_2 are inserted between the gate and the drain terminals of M13 and M12. The output stage dominant poles are located on the gates of M13 and M12 and have to be slowed down. The capacitors C_1 and C_2 can move these poles toward lower frequencies. This frequency compensation is more efficient because the capacitance effect is magnified by a factor of C_1/C_{gs} (of M13) or C_2/C_{gs} (of M12)[7].

A special effort was spent on this frequency compensation of the output stage. The whole amplifier is stabilized with the capacitor C_0, which is connected between IN- and V_{OUT}.

4 Other circuits

Some other circuits are included in the audio

power amplifier driving headphone. The bias circuit provides three voltage biases, and a row of resistances can be selected to serve as feedback resistance. ESD should be considered in this chip.

5 Conclusion

A low noise, low power, low distortion fully differential audio power amplifier with programmable gain for driving headphones has been presented. The system is based on an operational amplifier, which is discussed particularly. It has been implemented in a CSMC 0.6μm, 2 poly, 2 metal 5V CMOS process. The layout (including two audio amplifiers and digital controls) of the audio power amplifier is shown in Fig. 4. The nominal operating voltage for this chip is 5V, and it can operate from 2.5 to 5.5V. It obtains a 0.1% THD + N with 5V power-supply, a 1kHz frequency audio signal, and a 120mW continuous average output power into a 16Ω load. The gain can be set from + 12 to − 34.5dB in 32 discrete steps of 1.5dB. The specifications of the amplifier are summarized in Table 1.

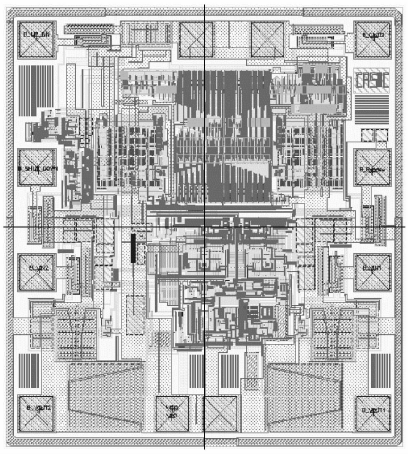

Fig. 4　Layout of the audio power amplifier

Table 1　Specifications of the amplifier

V_{DD} = 5V, T = 25℃	Measured
DC open loop gain	90dB
Phase margin	62°
Offset voltage	50μV(typical)
THD @ 1kHz	− 95dB
Power consume	1.2mA × V_{DD}
Area	0.65mm^2

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一款用于驱动耳机的低噪声低功耗音频功率放大器的设计

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摘要：报道了一款低噪声、低功耗、增益可调的音频功率放大器的设计. 该功率放大器在电源电压为 5V, 输入信号频率为 1kHz, 驱动负载为 16Ω, 输出功率为 120mW 时的总谐波失真仅为 0.1%. 此音频功率放大器的增益允许以每台阶为 1.5dB 在 + 12～ − 34.5dB 之间变化, 共 32 个台阶, 内部的放大器电路是该用于驱动耳机的音频功率放大器的核心. 介绍了功率放大器的电路结构、放大器的主要模块、最终版图和测试结果, 最后此电路在上华 0.6μm 双层多晶硅、双层金属的 CMOS 工艺上实现.

关键词：音频功率放大器；低噪声；低功耗

EEACC：1220；1280

中图分类号：TN402　　**文献标识码**：A　　**文章编号**：0253-4177(2006)S0-0029-03

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2005-10-11 收到, 2005-12-28 定稿