Comparison of Body-Contact and Patterned-SOI LDMOSFETs for RF Wireless Applications

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Abstract: A novel patterned-SOI LDMOSFET with a silicon window beneath the p-type channel is designed and fabricated for RF power amplifier applications. It has good DC and RF characteristics, with no kink effect on the output performance, an off-state breakdown of up to 13V, f_T = 8GHz at a DC bias of V_G = 4V and V_D = 3.6V. These characteristics are better than those of body-contact SOI LDMOSFETs on the same wafer with the same process conditions.

Key words: body-contact; patterned-SOI; LDMOSFET; RF
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1 Introduction

The lateral double-diffused MOSFET (LDMOSFET) has been a popular candidate in power amplifier applications. However, its high parasitic output capacitance and leakage current on bulk substrate result in lower power gain and power-aided efficiency. The silicon-on-insulator (SOI) LDMOSFET has much lower parasitic output capacitance and leakage current, making it a better candidate for high frequency applications[1~4]. However, the buried oxide layer induces a serious floating body effect in the partially-depleted SOI device, such as a kink in the *I-V* characteristics, which gives rise to distortion during power operation and produces poor power efficiency[5]. In addition, application of the SOI in a high-power-integrated circuit is limited by the self-heating effect caused by the poor thermal conductivity of the insulating SiO_2 layers.

Body-contact technology[5], shallow source implantation technology[6], and patterned-SOI technology[7,8] have been proposed to eliminate the floating body effect. However, the body-contact structure reduces gate width, and shallow source implantation requires careful process control, especially for a thin-film SOI structure. Ren *et al*.[7] fabricated a patterned-SOI LDMOSFET with no buried oxide beneath the source and p-type well regions, resulting in poor isolation between adjacent circuits. In addition, the process used to form patterned-SOI materials is too complex to be accepted widely. Park *et al*.[8] simulated a patterned-SOI structure with no buried oxide underneath the drain region, which increased the leakage current and parasitic output capacitance.

In this paper, a novel patterned-SOI (PSOI) LDMOSFET structure is proposed. The buried oxide is interrupted beneath the p-type well region, which is in a region called the silicon window. PSOI materials can be realized easily by masked SIMOX technology[9].

2 Device fabrication

The main processes used to form the PSOI/SOI materials on the same die are illustrated in Fig. 1. Thick thermal SiO_2 was grown on a p-type wafer (10 ~ 20Ω · cm) and etched selectively where the buried oxide layer was to be formed. Then the oxygen ion was implanted (low dose, 100keV, with an ULVACIM-200) and annealed (1300℃ for 5h). The thickness of the active silicon was about 0.2μm, the thickness of the buried oxide was about 0.1μm, and the length of the silicon window was about 0.8μm.

The PSOI and body-contact SOI LDMOS-

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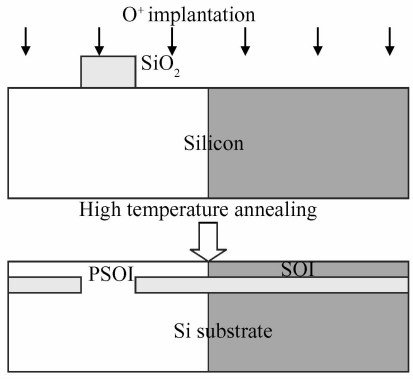

Fig.1　Local SIMOX process

FETs were fabricated simultaneously on the same die, compatible with a standard 1μm CMOS process. Each cell has 20 fingers with a 1μm gate and finger width, for a total gate width of 1mm (Fig.2). The gate oxide was thermally grown on the SOI wafer with a thickness of 30nm and a length of 1μm. Boron ions (1.5×10^{13} cm^{-2}, 35keV) were implanted into the source region and annealed for 2h at 1150℃ to form p-well doping. The length of the drift region was 0.5μm. The drift region doping was achieved by a blanket implantation of phosphorus (2×10^{12} cm^{-2}, 50keV) and annealing. Oxide was deposited by TEOS and was etched selectively to define the drift region and to form a spacer wall. After the source and drain regions were made by phosphorus ion implantation, a titanium silicide was performed.

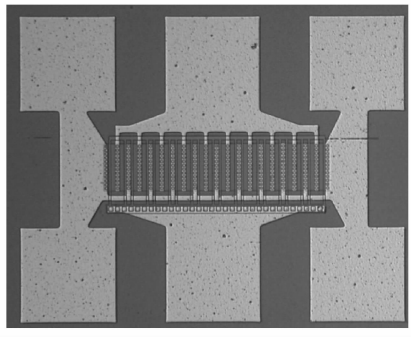

Fig.2　Image of the LDMOSFETs with GSG pad

3　Results and discussion

The devices were characterized on the wafer level by examining the DC *I-V* curves with an Agilent 4156C precision semiconductor parameter analyzer and the *S*-parameters with an Agilent E8363B PNA series network analyzer. The software we used includes ICCAP-2004 and ADS-2004A. Several differences are observed and corresponding reasons are explained in this section.

The transfer characteristics are shown in Fig. 3. The threshold voltage of the PSOI device is about 1.6V, which is 0.4V lower than that of the body-contact SOI LDMOSFET in the same B^+ implantation and annealing conditions because of the diffusion of the B^+ ions into substrate through the silicon window under the gate. As shown in Fig.3, we can conclude that the current drive ability by the gate voltage of the PSOI LDMOSFET is better than that of the body-contact SOI device due to the lower threshold voltage of the PSOI device and the reduction of the effective gate width for the p^+-type body-contact of the SOI LDMOSFET.

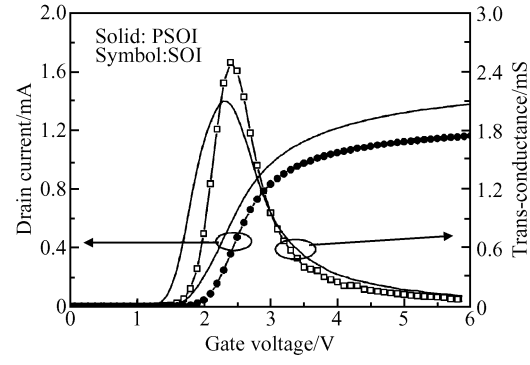

Fig.3　Transfer characteristics of the devices at V_D = 0.1V

The DC output characteristics are shown in Fig.4, in which the gate voltage varies from 2 to 5V by 0.5V steps. From Fig. 4, as Fig. 3, we can conclude that the PSOI LDMOSFET has better current drive ability by the gate voltage. For example, at the same bias condition as $V_G = V_D =$ 3V, the drain current of the PSOI LDMOSFET is 23mA, while that of the SOI device is only 7.2mA. The output characteristics curves in the saturation region of the PSOI LDMOSFET are very flat, proving that the floating body effect, like the kink effect, is eliminated by the novel PSOI structure we proposed, because the holes generated by the impact ionization in the neutral p-type region, can easily flow to the substrate through the silicon window. The on-state and off-state breakdown voltages of the PSOI LDMOS-

FET are 8 and 13V, respectively, which satisfy the requirements of the RF power amplifiers used in cell phones. We should explain that when the V_D rises to 5V, the output drain current of the PSOI device is locked to 0.1A for self-protection of the equipment.

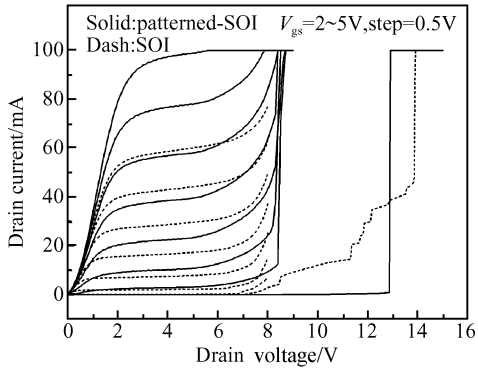

Fig. 4 DC output characteristics of the devices

The small signal characterization was performed using coplanar waveguide GSG probes. Calibration to the probe pads was obtained using a ceramic impedance standard substrate (ISS) and the short-open-load-thru (SOLT) method.

The *S*-parameters of the devices were measured to 10GHz. Figure 5 shows that the small signal voltage gain of the PSOI LDMOSFET is 6dB at 1GHz, which is better than that of the body-contact SOI device. Also, f_T was calculated by extrapolating at a slope of 20dB/Dec from H_{21} in Fig. 6. The f_T of the PSOI LDMOSFET is about 8GHz, greater than the value of 6GHz that was obtained for the body-contact SOI device.

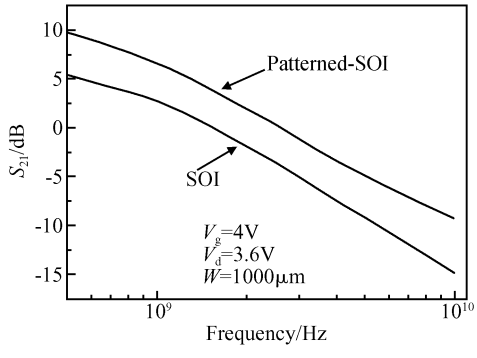

Fig. 5 S_{21} versus frequency of PSOI and SOI LDMOSFETs

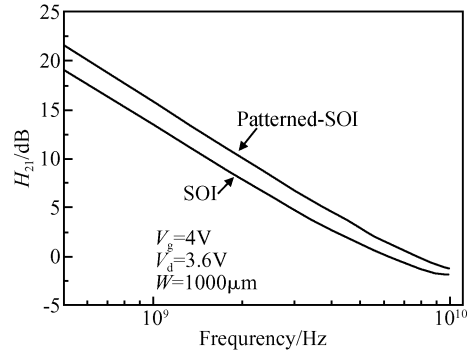

Fig. 6 H_{21} versus frequency of the devices

4 Conclusion

An RF power PSOI LDMOSFET was fabricated using masked SIMOX technology and a standard SOI CMOS process. This novel device has good DC and RF characteristics, with no kink effect on the output performance, an off-state breakdown of up to 13V, and f_T = 8GHz at a DC bias of V_G = 4V and V_D = 3.6V. This is a promising technology for RF PAs in the future generations of highly integrated wireless systems.

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射频无线应用的体连接和图形化 SOI LDMOSFET 的比较

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摘要：设计并制作了一种可应用于无线通信放大器的新型的图形化 SOI LDMOSFET.该器件沟道下方的埋氧层是断开的.测试表明,输出特性曲线没有发现明显的翘曲效应,关态的击穿电压达 13V,在 $V_G = 4V$ 和 $V_D = 3.6V$ 时 f_T 为 8GHz,直流和射频性能均优于同一芯片上相同工艺条件制备的体接触 LDMOSFET.

关键词：体接触；图形化 SOI；LDMOSFET；射频
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