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A Model of the Temperature Dependence of the Fall Time of a TF SOI CMOS Inverter with EM NMOST and AM PMOST Assemblies at 27～300℃ *

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Abstract: The temperature dependence of the fall time of an SOI CMOS inverter with EM NMOST and AM PMOST assemblies is modeled approximately in electronics in a high temperature range (27～300℃) in detail. In addition, experiments on the inverter are done at 27, 100, 150, 200, 250, and 300℃, respectively, and the measured results are illustrated and discussed simply. They indicate that the inverter is very suitable for high temperature applications up to 300℃ and that its fall time varies only slightly with temperature. If optimization is introduced during its design process, a more symmetrical rise/fall characteristic may be realized, and it could be used at higher frequencies.

Key words: SOI; CMOS; high temperature; model; fall time
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1 Introduction

SOI CMOS circuits are suitable for high-temperature applications because of their inherent reduction in junction leakage current related to that in bulk-silicon devices. The fall time of SOI CMOS inverters is an important parameter to be considered in the design of SOI VLSI/ULSI systems and smart power ICs operating at elevated temperatures. Although much work on SOI MOSTs operating at high temperatures has been reported[1～9], there have been only a few reports about the fall time of SOI CMOS inverters[10～13], and in these reports the fall time is not modeled in enough detail. In this paper, the temperature dependence of the fall time of SOI CMOS inverters with EM NMOST and AM PMOST assemblies is modeled approximately in electronics in a high temperature range (27～300℃) in detail. In addition, experiments on the inverter are done at 27, 100, 150, 200, 250, and 300℃, respectively, and the measured results are discussed.

2 Fall time of the TF SOI CMOS inverter t_f

The fall time of a TF SOI CMOS inverter can be defined as the time that it takes the output voltage V_o to rise from $0.9V_{dd}$ to $0.1V_{dd}$ at an ideal step stimulus. The falling process equivalent circuit is shown in Fig. 1, in which V_{dd} represents the supply voltage. For convenience in our analysis, we neglect the influences of the response time and the leakage current of the MOSTs, the parasitic capacitances at the output terminal, and the interconnect wires. Furthermore, we suppose that the load capacitance C_L is independent of temperature. Therefore C_L can be expressed approximately as

$$C_L \approx C_{ox1} W_n L_n + C_{ox1} W_p L_p \qquad (1)$$

where C_{ox1} is the capacitance density of the forward gate oxide capacitor, W_n and L_n are the channel width and length of the NMOST, and W_p and L_p are the channel width and length of the PMOST, respectively.

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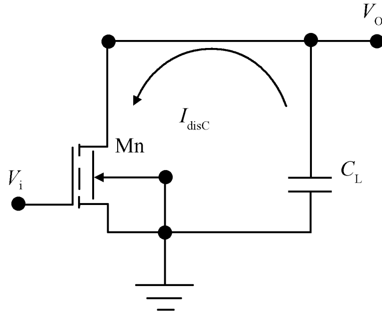

Fig. 1 Falling process equivalent circuit of NMOST of TF SOI CMOS inverter

As the ideal step stimulus jumps from logic "0" to "1", the PMOST is turned off, while the NMOST operates in the strong inversion state. At the same time, the power supply is turned off by the PMOST, while the C_L begins to be discharged through the NMOST to the ground. During the discharge process, the NMOST experiences two different states. One is a saturation state and the other is a non-saturation state. Therefore the fall time includes two phases, which we call the 1st fall time t_{f1} and the 2nd fall time t_{f2}.

2.1 1st fall time t_{f1}

When $V_o \in [V_{dd} - V_{TN}, V_{dd}]$, the NMOST is saturated, and the charge equation can be expressed according to the gradual channel approximation as

$$C_L \frac{dV_o}{dt} = \frac{1}{2} \times \frac{K_N}{1 + C_r}(V_{dd} - V_{TN})^2 \qquad (2)$$

where V_{TN} is the threshold voltage of the NMOST, which decreases as the temperature increases[4]; C_r is the ratio between the capacitances at the forward interface, which can be expressed as $C_r = C_{Si} C_{ox2} / C_{ox1}(C_{Si} + C_{ox2})$, where C_{Si} represents the surface capacitance density of the SOI film and C_{ox2} represents the BOX capacitance density; and the coefficient K_N can be expressed as[3]

$$K_N = \frac{\mu_{sn} C_{ox1} W_n}{L_n} \qquad (3)$$

where μ_{sn} is the surface mobility of an electron, which decreases as the temperature increases. Thus t_{f1} is the time that it takes V_o to fall from $0.9V_{dd}$ to $V_{dd} - V_{TN}$.

$$t_{f1} = \frac{2(1 + C_r)C_L}{K_N(V_{dd} - V_{TN})^2}\int_{V_{dd}-V_{TN}}^{0.9V_{dd}} dV_o = \frac{2(1 + C_r)C_L(V_{TN} - 0.1V_{dd})}{K_N(V_{dd} - V_{TN})^2} \qquad (4)$$

2.2 2nd fall time t_{f2}

When $V_o \in [0.1V_{dd}, V_{dd} - V_{TN}]$, the NMOST becomes non-saturated, and the discharge equation can be expressed as

$$C_L \frac{dV_o}{dt} = -K_N\left[(V_{dd} - V_{TN})V_o - (1 + C_r)\frac{V_o^2}{2}\right] \qquad (5)$$

Suppose t_{f2} is the time that it takes V_o to fall down from $V_{dd} - V_{TN}$ to $0.1V_{dd}$. Then we can obtain

$$t_{f2} = \frac{C_L}{K_N}\int_{0.1V_{dd}}^{V_{dd}-V_{TN}}\left[(V_{dd} - V_{TN})V_o - \frac{1 + C_r}{2}V_o^2\right]^{-1} dV_o = \frac{C_L}{K_N(V_{dd} - V_{TN})}\ln\frac{(19 - C_r)V_{dd} - 20V_{TN}}{(1 - C_r)V_{dd}} \qquad (6)$$

2.3 Fall time t_f

Based on the above discussion, the fall time of the TF SOI CMOS inverter operating in a high temperature range can be derived as the sum of t_{f1} and t_{f2}:

$$t_f = t_{f1} + t_{f2} = \frac{2(1 + C_r)C_L(V_{TN} - 0.1V_{dd})}{K_N(V_{dd} - V_{TN})^2} + \frac{C_L}{K_N(V_{dd} - V_{TN})}\ln\frac{(19 - C_r)V_{dd} - 20V_{TN}}{(1 - C_r)V_{dd}} = \frac{C_L}{K_N(V_{dd} - V_{TN})}\left[\frac{2(1 + C_r)(V_{TN} - 0.1V_{dd})}{V_{dd} - V_{TN}} + \ln\frac{(19 - C_r)V_{dd} - 20V_{TN}}{(1 - C_r)V_{dd}}\right] \qquad (7)$$

3 Experiments and results

A TF SOI CMOS inverter with EM NMOST and AM PMOST assemblies is chosen as the sample with the following main parameters: $t_{Si} = 120 \pm 20$nm, $N_A = 2 \times 10^{16}$ cm^{-3}, $t_{oxf} = 40$nm, $t_{oxb} = 380$nm, $N_{sub} = 8 \times 10^{14}$ cm^{-3}, $N_{poly} = 1 \times 10^{21}$ cm^{-3}, $L = 3\mu$m, $W_p = 40\mu$m, $W_n = 20\mu$m. A dual-channel oscillator, a high precision digital camera connected to a computer, a high temperature chamber, and some heat-resistant wires were used in the experiments at 27, 100, 150, 200, 250, and 300℃, respectively. During the experiments, the supply voltage was set at 5V. The substrates of both MOSTs and the source of the NMOST were connected to ground. The measured results are shown in Fig. 2[13].

It can be seen from Fig. 2 that there are at least four features:

(1) The inverter performed very well up to 300℃ mainly because the EM NMOST and the

AM PMOST match well and are very suitable for high temperature applications.

(2) The fall time is shorter than the rise time because the ratio of width to length of the two MOST channels is less than that of the electron mobility to the hole mobility, and the threshold voltage of the NMOST V_{TN} is less than $|V_{TP}|$, and so the drain current value of the NMOST is larger than that of the PMOST.

(3) Since the voltage between the gates cannot be changed abruptly and the state of SOI film changes more slowly than the input signal, the peak voltages can be observed in the photos.

(4) The fall time increases only slightly as the temperature increases because, as can be seen from Eq.(7), V_{TN} and $|V_{TP}|$ decrease with temperature, and so the drain currents increase with temperature, which compensates the influence from the decrease of the carrier mobilities with temperature to some extent.

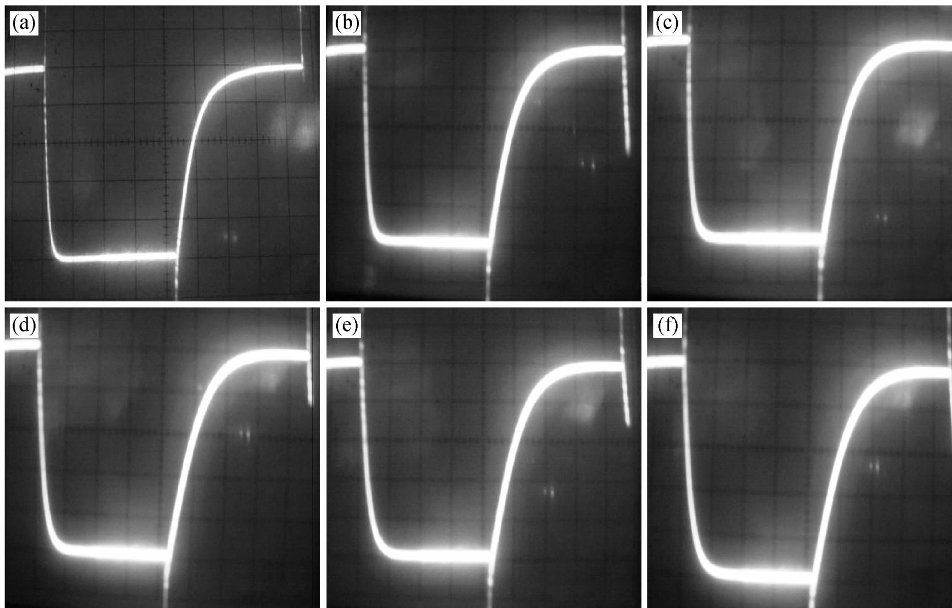

Fig.2 Transient characteristic of TF SOI CMOS inverter with EM NMOST and AM PMOST assemblies (x: 5μs/div; y: 1V/div) (a) 27℃; (b) 100℃; (c) 150℃; (d) 200℃; (e) 250℃; (f) 300℃

4 Conclusion

The measurements mentioned above show that the TF SOI CMOS inverter with EM NMOST and AM PMOST assemblies is suitable for high temperature applications up to 300℃, and its fall time varies only slightly with temperature. If it is designed optimally, a more symmetric fall-down/rise-up characteristic may be realized and it could be used at higher frequencies.

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EM NMOST 和 AM PMOST 组合 TF SOI CMOS 非门下降时间的温度模型*

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摘要：详细介绍了 EM NMOST 和 AM PMOST 组合的 TF SOI CMOS 非门下降时间的温度电学模型建立过程.分别进行了 27,100,150,200,250,300℃的非门瞬态特性实验.实验结果表明,EM NMOST 和 AM PMOST 组合的 TF SOI CMOS 非门的下降时间随温度升高稍有增加,非常适合于高温应用.如果对其进行优化设计,有利于改善其上升-下降时间温度特性的对称性,提高其最高工作频率.

关键词：绝缘层上硅；CMOS；高温；模型；下降时间

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