Design Issues for Cross-Coupled LC Oscillators

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Abstract: This paper introduces design issues for cross-coupled LC oscillators. From a physical standpoint, the VCO topology, the amplitude of the tank, the noise source, the phase noise, and the Q factor of the tank are studied. According to these analyses, the design issues and constraints are presented. Finally, the simulation results of a cross-coupled LC oscillator are reported.

Key words: integrated LC VCO; on-chip spiral inductor; phase noise
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1 Introduction

The integrated LC voltage-controlled oscillator (VCO) is a common functional block in modern radio frequency communication systems and is used as a local oscillator to upconvert and downconvert a signal. Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators. Much effort[1~3] has been made to improve the phase-noise performance of integrated LC VCOs. Despite of these endeavors, the design and optimization of integrated LC VCOs still pose many challenges to circuit designers.

Here we study LC oscillators from a physical standpoint. Several essential insights about the noise characteristics are provided. A specific oscillator topology is chosen as a design example, and design considerations are also presented.

2 Physical points of LC VCOs

In this section, we simply analyze the noise of an LC VCO and introduce a linear time-variant (LTV) phase-noise model.

2.1 LC VCO topology

The cross-coupled LC oscillator shown in Fig. 1 is selected as the object of our research. This topology has good properties. The full exploitation of the differential operation reduces undesirable common-mode effects. The amplitude of this structure is larger than that of the nMOS-only structure due to the pMOS pair. The rise and fall time symmetry is also incorporated to further reduce the $1/f$ noise upconversion. All these result in a better phase-noise performance for a given tail current.

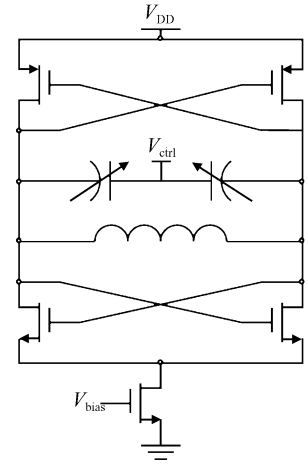

Fig. 1 Schematic of an LC VCO

2.2 Tank voltage amplitude

Figure 2 shows a model of a parallel LC oscillator in the steady state, where R is the resistor of the resonator and $-R_a$ is the effective negative resistor of the active device. At the resonance frequency, the admittances of the L and C cancel, leaving R. The tank amplitude can be approximated as

$$V_{tank} \approx I_{tail} R \tag{1}$$

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According to Ref. [5], there are two operation modes, which are called the current-limit regime and the voltage-limit regime. Equation (1) is valid only in the current-limit regime where the amplitude is proportional to the tail current. When the oscillator enters the voltage-limit regime, the amplitude is limited to $V_{\max}$.

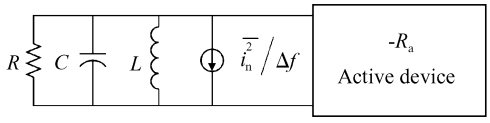

Fig. 2 Parallel LC oscillator model

2.3 Noise source

There are three noise sources: drain current noise, inductor noise, and varactor noise. They are given by

$$\frac{\overline{i_{\text{MOS}}^2}}{\Delta f} = 4kT\gamma g_{\text{active}} \tag{2}$$

$$\frac{\overline{i_{\text{ind}}^2}}{\Delta f} = 4kTg_{\text{L}} \tag{3}$$

$$\frac{\overline{i_{\text{var}}^2}}{\Delta f} = 4kTg_{\text{var}} \tag{4}$$

where γ is 2/3 and 2.5 for long- and short- channel transistors, respectively.

Considering the start-up condition and the worst-case condition, we can obtain

$$g_{\text{active}} \geqslant \alpha g_{\text{tank,max}} \tag{5}$$

where α is the minimum small-signal loop gain. To make sure that the circuit can oscillate, we should select a conservation value of 2.5 or larger. According to Eqs. (2)~(5), an inequality is given by

$$\frac{\overline{i_{\text{ind}}^2}/\Delta f + \overline{i_{\text{var}}^2}/\Delta f}{\overline{i_{\text{MOS}}^2}/\Delta f} < \frac{4kTg_{\text{tank,max}}}{4kT\gamma g_{\text{active}}} \leqslant \frac{1}{\gamma\alpha} \tag{6}$$

The inequality predicts that the four cross-coupled transistors contribute more than 84% of the circuit noise for short-channel transistors. Hence we can obtain

$$\frac{\overline{i_{\text{n}}^2}}{\Delta f} \approx 4kT\gamma g_{\text{active}} \tag{7}$$

2.4 Phase-noise analysis

According to the Hajimiri model[4], we can obtain phase-noise of LC oscillators in the $1/f^2$ region and phase-noise in the $1/f^3$ region

$$L(\Delta\omega) = \frac{\Gamma_{\text{rms}}^2}{q_{\max}^2} \times \frac{\overline{i_{\text{n}}^2}/\Delta f}{2\Delta\omega^2} \tag{8}$$

$$L(\Delta\omega) = \frac{c_0^2}{q_{\max}^2} \times \frac{\overline{i_{\text{n,1/f}}^2}/\Delta f}{8\Delta\omega^2} \tag{9}$$

where Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with the noise source, $q_{\max}$ is the maximum charge displacement across the capacitor, $\overline{i_{\text{n}}^2}/\Delta f$ is the noise power spectral density due to transistor noise, inductor noise, and varactor noise, and $\overline{i_{\text{n,1/f}}^2}/\Delta f$ is the noise power spectral density due to transistor flicker noise.

According to analysis of the LC oscillator model, we can obtain

$$q_{\max} = C_{\text{tank}} V_{\text{tank}} = \frac{I_{\text{tail}} Q_{\text{tank}}}{\omega_0} \tag{10}$$

Therefore, from Eqs. (7)~(10), we obtain the approximate relation

$$L(\Delta\omega) \propto \frac{1}{I_{\text{tail}}^2 Q_{\text{L}}^2} \times g_{\text{active}} \tag{11}$$

As can be seen from Eq. (11), a larger tail current results in a better optimum phase noise. Hence the tail current should always be set to its maximum value allowed by other design constraints. Increasing the tank Q factor is another way to reduce phase noise.

2.5 Q factor of tank

As shown in Fig. 2, R is the equivalent parallel resistor of the tank. In CMOS technology, the Q_{L} factor of the on-chip inductor is from 5 to 10, and the Q_{C} factor of the varactor is more than 20. Therefore, we obtain the approximation

$$R \approx \frac{\omega_0 L Q_{\text{L}} Q_{\text{C}}}{Q_{\text{L}} + Q_{\text{C}}} \tag{12}$$

Then, the Q factor of the tank is given by

$$Q_{\text{tank}} = \sqrt{\frac{R^2 C}{L}} = \frac{Q_{\text{L}} Q_{\text{C}}}{Q_{\text{L}} + Q_{\text{C}}} \tag{13}$$

Since

$$Q_{\text{C}} \gg Q_{\text{L}}, Q_{\text{tank}} \approx Q_{\text{L}} \tag{14}$$

As can be seen from Eq. (14), increasing the Q factor of the inductor results in a larger Q factor of the tank. Thus the on-chip inductor must be designed carefully.

3 LC oscillator design

In section 2, the underlying physical factors were discussed. In this section, design issues for a cross-coupled LC oscillator are discussed. The design is based on 0.25μm 1P5M RF CMOS technology.

3.1 Phase-noise and power

For a given supply voltage, a larger tail current results in a larger power dissipation. Although larger power dissipation means a better phase-noise, in most cases the power should be as small as possible. We must balance phase-noise and power dissipation.

Figure 3 shows the simulated LC oscillator phase-noise as a function of the tail current for 2.5V V_{DD}.

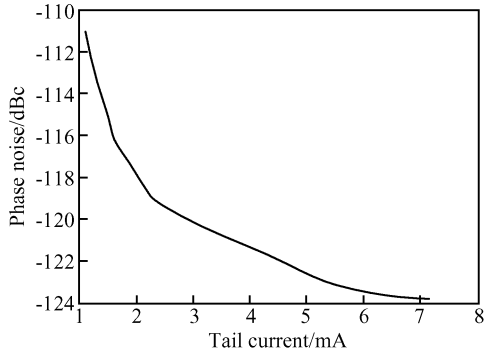

Fig. 3 Phase noise versus tail current

As can be seen from Fig. 3, when the tail current is small, the phase-noise improves markedly as the tail current increases. When the tail current is larger than a certain value, the phase-noise is almost constant. The simulated result is consistent with Eq. (11).

According to the above results, the best range of tail current, where the phase-noise and power dissipation are balanced well, is from 3 to 5mA. Considering the power dissipation, 4mA is selected as a good tradeoff in our design.

3.2 On-chip spiral inductor

The on-chip spiral inductor is a critical component that determines the phase-noise of an LC oscillator. The Q factor of an on-chip spiral inductor should be as large as possible to increase the Q factor of the tank. Due to four mechanisms, which include the skin effect, eddy current, metal resistance, and substrate-induced loss, the Q factor for a spiral inductor is typically below 10.

Considering the resistance and skin effect, the metal depth should be equal to the skin depth[6].

$$\delta_{\text{depth}} = \sqrt{\frac{2}{\omega\mu_0\sigma}} \tag{15}$$

Here σ is the conductivity of the metal, and μ_0 is the permittivity in vacuum.

Considering the eddy current and substrate-induced loss, the dimension of the spiral inductor, including metal width, metal spacing, number of turns, and diameter, should be designed carefully and the inductor must remain hollow.

3.3 Varactor

In CMOS technology, there are two types of varactors: the pn junction varactor and the MOS varactor. The latter is more popular in LC oscillator design because of its large tuning range.

Constrained by the center frequency and frequency tuning range, the value of the varactor must satisfy these inequalities:

$$C_{\text{tank,min}} \leqslant \frac{1}{L_{\text{tank}}\omega_{\max}^2} \tag{16}$$

$$C_{\text{tank,max}} \geqslant \frac{1}{L_{\text{tank}}\omega_{\min}^2} \tag{17}$$

Here C_{tank} represents the equivalent parallel capacitance of the tank due to the varactors, load capacitances, and parasitic capacitances of the MOS transistors.

3.4 Dimensions of transistors

To satisfy the start-up conditions, the admittance of transistors must be large enough. However, large transistors have their drawbacks. For a given tail current, the larger the admittance of the transistor is, the smaller the output voltage swing is. If the output swing is too small, the next stage cannot work correctly. According to the model of transistors[7], the flick noise is given by

$$\frac{\overline{i_{\text{n},1/f}^2}}{\Delta f} = \frac{K}{C_{\text{ox}}WL} \times \frac{1}{\Delta f} g_{\text{MOS}}^2 \propto \frac{W}{L^3} \times \frac{1}{\Delta f} \tag{18}$$

A large g_{MOS} means that the cross-coupled transistors contribute more flick noise in the $1/f^3$ region and more drain current noise in the $1/f^2$ region. These result in another tradeoff in the LC oscillator design.

3.5 Optimization phase noise

According to the above analyses, three design issues for optimizing phase noise are presented:

(1) Increasing the tail current can lower the phase-noise of an LC oscillator. Hence the tail

current should always be set to its maximum value allowed by the other design constraints.

(2) Increasing the Q factor of the on-chip spiral inductor can lower the phase-noise of an LC oscillator.

(3) Reducing the W of the transistors can lower the flick noise and drain current noise of the transistors. However, the start-up condition must be satisfied.

4 Conclusion

In this paper, issues in the design of LC oscillators have been presented. These issues include the following: designing an on-chip spiral inductor with a high Q factor; balancing the phase noise and power dissipation and selecting the value of the tail current; calculating the value of the varactor; and designing the dimensions of the transistors.

Using the methods mentioned above, a 2.4GHz cross-coupled LC oscillator is designed with 0.25μm 1P5M RF CMOS technology. Figure 4 shows the core layout of the LC oscillator. The simulation results are as follows. The phase noise is -114.4dBc at 600kHz. The power dissipation is 10.5mW for a 2.5V supply. The tuning range is 6%.

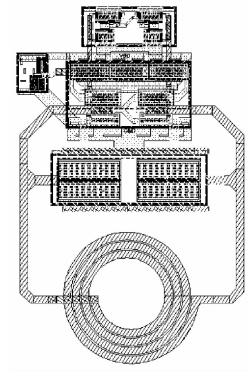

Fig.4 Layout of VCO core

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LC 振荡器的设计要点

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摘要: 主要介绍了 LC 振荡器的设计要点.从 LC 振荡器的模型出发,研究了 VCO 的电路结构、谐振回路对于输出幅度的影响、VCO 的噪声源、VCO 的相位噪声以及谐振回路的 Q 值对于 VCO 的影响.给出了 LC 振荡器的设计要点及设计中需要考虑的约束条件.

关键词: 集成 LC VCO; 片上螺旋电感; 相位噪声

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