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3-D Simulation of FINFET*

Liu Enfeng, Liu Xiaoyan and Han Ruqi

(*Institute of Microelectronics, Peking Universtiy, Beijing* 100871, *China*)

Abstract: An SOI MOSFET with FINFET structure is simulated using a 3-D simulator. I-V characteristics and sub-threshold characteristics, as well as the short channel effect (SCE) are carefully investigated. SCE can be well controlled by reducing fin height. Good performance can be achieved with thin height, so fin height is considered as a key parameter in device design. Simulation results show that FINFETs present performance superior to conventional single gate devices.

Key words: FINFET; 3-D simulation; short channel effect
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1 Introduction

According to Moore's law, MOSFET have been scaled down to nanometer regime with good performance at low cost. However, it is reported that conventional technology will face big challenge when gate length scaling down to 35nm[1]. In order to maintain present IC industry, various technologies have been achieved, such as high-k dielectrics, channel engineering and novel device structure. Among them, SOI double gate device may be the most attractive one[2]. It has demonstrated that double gate devices show better performance than conventional single gate devices. Double gate devices have introduced the concept of volume inversion layer, that is, the minority carriers are no longer confined to a single interface, but spread over the whole device if the width is thin enough[3]. Recently, a double gate SOI MOSFET-FINFET with 18nm gate length was reported by Hu's group[4,5]. This structure shows good compatibility with conventional CMOS technology, and has presented good performance comparing with bulk silicon devices, such as thin fin for suppression of short channel effect, self-aligned double gate, reduced parasitic effects, and quasi-planar topography[4,5]. This can be considered as an attractive direction for CMOS technology. Due to the reasons mentioned above, many investigations have been carried out, from device structure to simulation. Among these studies, the simulation is usually carried out under 2-D situation, 3-D effects are seldom reported.

In this paper, characteristics of FINFET are studied carefully by a 3-D simulator (DAVINCI[6]), which takes into account non local/stationary effect in ultra-deep sub-micron devices by solving Possion, continuity, energy-balance equation simultaneously. I-V characteristics and

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Liu Enfeng male, was born in 1973, PhD candidate. His research interests include device modeling and simulation.
Liu Xiaoyan female, associate professor. She has been engaged in the research on the novel device structure, device simulation and modeling.
Han Ruqi male, professor. His research interests are in the structures, modeling, and fabrication technologies of the novel semiconductor devices with nanoscale.

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subthreshold characteristics, as well as the short channel effect are investigated in details.

2 Device structure

Figure 1(a) shows the simulated FINFET device structure. The central part of the device is ultra thin silicon body and known as "fin"[7]. The channel which is formed on the surface of the fin and the gate is around the fin for three surfaces[4]. In the following sections, fin length will along x direction as shown in Fig. 1(a), width along z direction, height along y direction. Fig. 1(b) shows the top-view of Fig. 1(a). The source and the drain region are heavily doped n-type Si with dopant of $1\times10^{20}\mathrm{cm}^{-3}$. The length and width of the fin are 25 and 15nm, respectively, and fin height will vary from 10nm to 50nm for comparison.

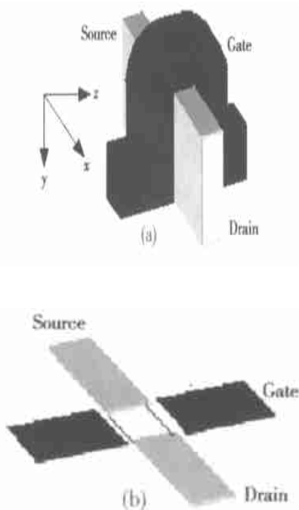

Fig. 1 (a) 3-D structure of FINFET[7]; (b) 2-D structure of FINFET (top-view of Fig. 1(a))[7]

3 Simulation results and discussion

The 3-D simulated results of the typical I-V characteristics of FINFET with substrate doping at $1\times10^{18}\mathrm{cm}^{-3}$ and $L=25\mathrm{nm}$, $W=15\mathrm{nm}$, $H=10\mathrm{nm}$ are shown in Fig. 2(a) and (b). The difference of I_{ds}-V_{gs} characteristics between 2-D (xz plane in Fig. 1(a)) and 3-D situation is compared in Fig. 2(b).

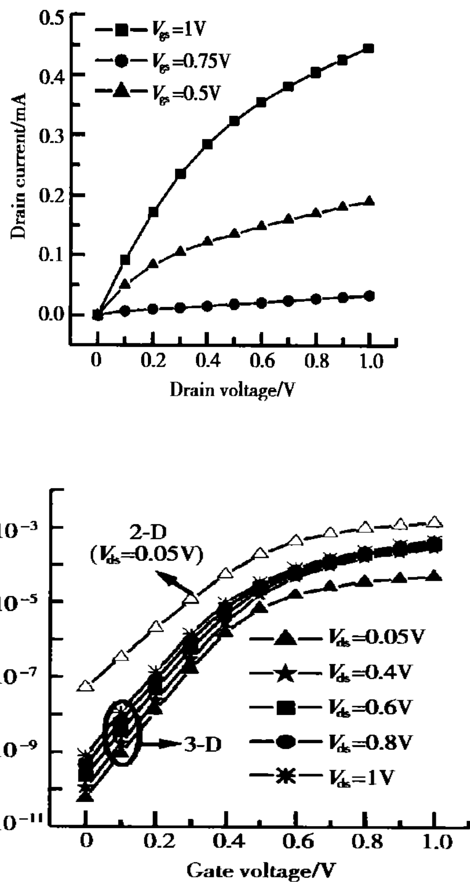

Fig. 2 (a) I_{ds}-V_{ds} characteristics with $L_{gate}=25\mathrm{nm}$, $W_{fin}=15\mathrm{nm}$, $H_{fin}=10\mathrm{nm}$; (b) I_{ds}-V_{gs} characteristics with $L_{gate}=25\mathrm{nm}$, $W_{fin}=15\mathrm{nm}$, $H_{fin}=10\mathrm{nm}$

From the figure, it can be seen that there exists obviously difference between the 2-D results and 3-D results. FINFET is a kind of novel structure with its scales of length, width and height very similar, and 3-D effect serious. However, previous simulation results were mainly based on two dimensions[4,5], that is, on the xz plane, the influences from the length and width of the fin can be carefully investigated, but the influences from height of fin can not be included. By using the 3-D device simulator, the 3-D effect of FINFET can be studied, and the influence of fin height can be investigated. Figure 3 shows the dependence of threshold voltage V_{th} and sub-threshold swing S on fin height. From figure 3 it can be seen that V_{th} increases and S decreases with decrease of fin height. This is because carriers in a lower body can

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be better controlled than that in a higher one. Moreover, it is easier to obtain volume inversion in a lower body. Thus sub-threshold characteristics of FINFET can be improved by reduced fin height.

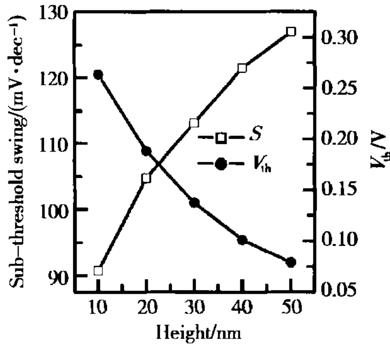

Fig. 3　Change of threshold voltage and sub-threshold swing with fin height with L_{gate} = 25nm, W_{fin} = 15nm

3-D simulation also indicates that fin height can influence the short channel effect of FINFET. To study the drain-induced barrier lowing effect (DIBL), an linear formula is adopted to fit the V_{th}[8].

$$V_{th} = V_{th0} - \sigma V_{ds}$$

where V_{th0} is defined as the threshold voltage when source-drain bias equals zero; σ is a constant parameter and known as DIBL coefficient. Figure 4 shows σ dependence on fin height, σ increases with

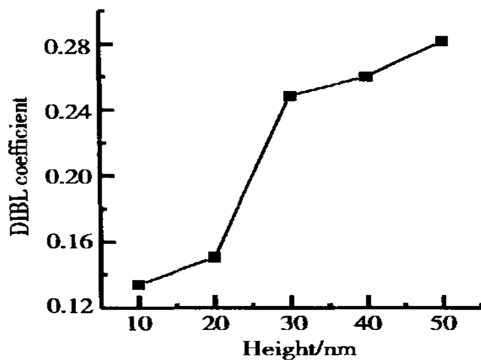

Fig. 4　DIBL coefficient dopendence on fin height with L_{gate} = 25nm, W_{fin} = 15nm

increasing fin height. Then the short channel effect can be suppressed by decreased fin height. Hence lower fin body will be a good choice if technology allows.

The fin height can influence the drain current due to its changing the cross section area of the channel. The I-V curves dependence of fin height for gate length of 100nm are shown in Fig. 5. As can be seen that fin height increases by five times, but saturation current only increase twice. This indicates that concentration of inversion carriers under gates can not increase linearly with the variation of channel section area.

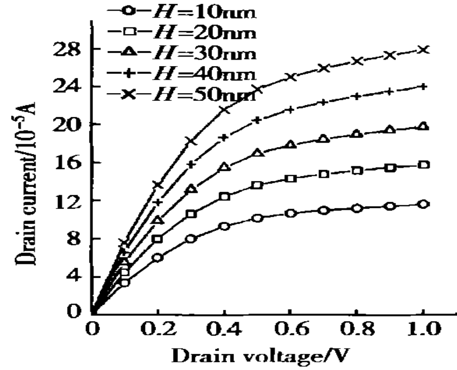

Fig. 5　I_{ds}-V_{ds} characteristics with different fin hight (L_{gate} = 100nm, W_{fin} = 50nm)

This can be explained by that electric field far away from the top gate and drain is lower than that near the top gate and drain, so the concentration of inversion carriers is lower when they are far away from the top gate. Furthermore, they are only the minor part of the total inversion carriers. When the fin height increases, only this minor part increases, it has less influence on the whole current. The saturation current can not increase linearly with the increase of the fin height. From 3D simulating results, we can find that device characteristics can be improved with reduced fin height without decreasing the driving current seriously. The high channel doping concentration is usually required to suppress the short-channel effect (SCE) in conventional MOSFETs. The sub-threshold swing and V_{th} dependence on different channel doping concentration are illustrated in Fig. 6. As can be seen in this figure, when the channel doping change from intrinsic to 1×10^{18} cm^{-3}, the threshold voltage only decreased by about 18mV and sub-threshold swing only increase

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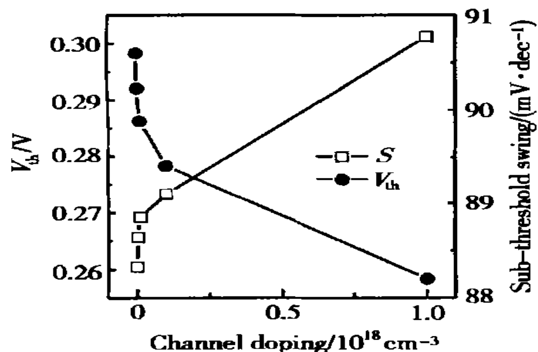

Fig.6 Change of threshold voltage and sub-threshold with channel doping ($L_{gate}=25$nm, $W_{fin}=15$nm, $H_{fin}=10$nm)

by about 36mV/dec. Hence the subthreshold characteristics of FINFET is less sensitive to the channel doping. Figure 7 shows the dependence of DIBL coefficient σ on substrate doping. From this figure, with the channel doping changing from intrinsic to 1×10^{18}cm^{-3}, σ only decreased by 0.021 (0.155 to 0.134). Though σ increases with the decrease of doping concentration, the values are insensitive to the channel doping, which means SCE is still not obvious in FINFET even with low channel doping concentration or intrinsic substrate. Thus light channel doping or even intrinsic substrate can be adopted in FINFET in order to suppress the doping fluctuation without sacrificing the device characteristics seriously.

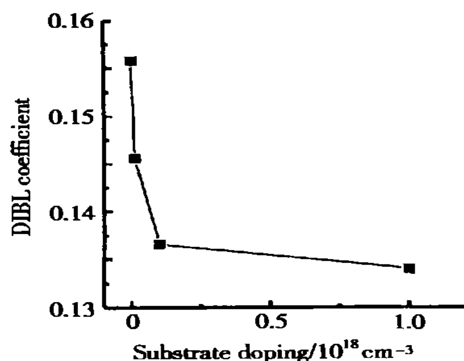

Fig.7 DIBL coefficient dependence on channel doping with $L_{gate}=25$nm, $W_{fin}=15$nm, $H_{fin}=10$nm

4 Conclusion

The characteristics of FINFET especially 3-D effects are studied carefully by 3-D numerical simulation. The influences from fin height and channel doping are investigated in details. The 3-D simulating results indicate that good sub-threshold characteristics and short channel effect can be achieved with the decrease of fin height, while saturation current decreases only twice with decrease of fin height for five times, which means that fin height has a significant effect on the device characteristics. The 3-D simulating results indicate that sub-threshold characteristics and short channel effect have less sensitive to the channel doping. The light channel doping or even intrinsic substrate can be adopted in FINFET in order to suppress the doping fluctuation without sacrificing the device characteristics seriously. These features make FINFET an attractive candidate for future CMOS technology, especially when gate length scaled down to 25nm generation.

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FINFET 的三维模拟*

刘恩峰　刘晓彦　韩汝琦

(北京大学微电子所，北京　100871)

摘要: 采用三维模拟软件对具有FINFET 结构的SOI-MOSFET 进行了模拟. 研究了FINFET 的 *I-V* 特性、亚阈值特性、短沟道效应等. 模拟发现，通过降低fin 的高度可以有效地抑制短沟道效应与提高器件的性能，因此fin 的高度是器件设计中一个关键参数. 模拟结果表明FINFET 在特性上优于传统的单栅器件.

关键词: FINFET；三维模拟；短沟道效应

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刘恩峰　男，1973 年出生，博士研究生，主要从事半导体器件的模型与模拟的研究工作.

刘晓彦　女，副教授，主要从事新器件的设计、半导体器件的模型与模拟的研究工作.

韩汝琦　男，教授，主要从事新器件的设计、纳米半导体器件的工艺及模型与模拟研究工作.

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