Study of Multiple SiGe/Si Layers Epitaxy and Selective Etching for High Performance Dynamic Random Access Memory(DRAM) Application

Zhenzhen Kong1,4, Hongxiao Lin3,4, Hailing Wang2, Yanpeng Song2, Junjie Li1, Xiaomeng Liu2, Yuanhao Miao1,3, Yiwen Zhang1,4, Yuhui Ren1,4, Chen Li 1,4, Jiahan Yu1,4, Jinbiao Liu1,4, Jingxiong Liu1,4, Qinzhu Zhang1, Jianfeng Gao1, Huihui Li2, Xiangsheng Wang2,Junfeng Li1, Anyan Du1, Henry H. Radamson3, Chao Zhao2, Tianchun Ye1,4, Guilei Wang2,5[†]

[1]Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China;

[2]Beijing Superstring Academy of Memory Technology, Beijing 100176, China;

[3]Research and Development Center of Optoelectronic Hybrid IC，Guangdong Greater Bay Area Institute of Integrated Circuit and System，Guangdong，510535, China;

[4]Microelectronics Institute, University of Chinese Academy of Sciences, Beijing 100049, China;

[5]Hefei National Laboratory, Hefei 230088, P. R. China

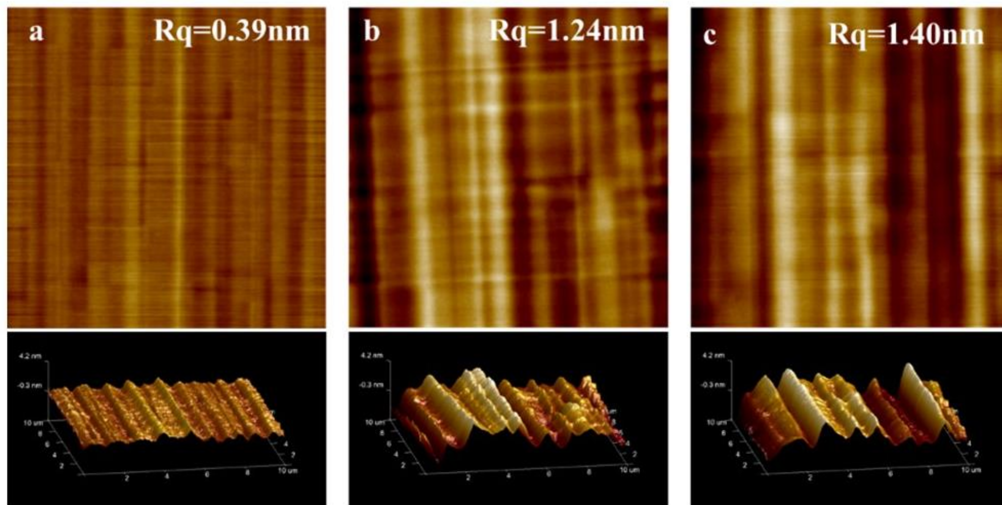

Fig. S1. The roughness and Rq of different thickness multilayers. (a) SiGe (20 nm) /Si MLs structure; (b) SiGe (40 nm) / Si MLs structure; (c) SiGe (60 nm) / Si MLs structure.[1]

† Correspondence to: Guilei Wang, Email: Guilei.Wang@bjsamt.org.cn

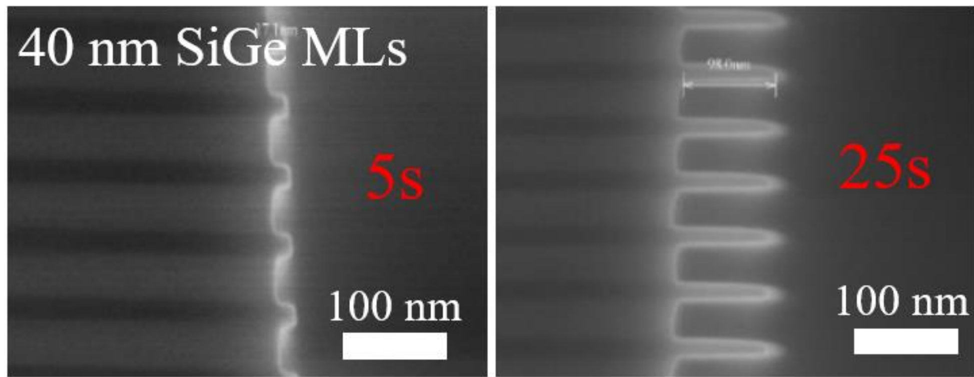

Fig. S2. The SEM profile of SiGe(40nm) / Si MLS structure after 5s and 25s lateral etch.

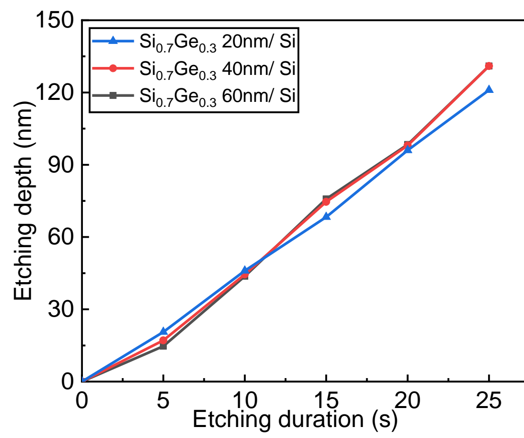

Fig. S3. The etch rate of lateral dry etching for three MLs structures.