A Wide-Band Low Noise Amplifier for Terrestrial and Cable Receptions *

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Abstract: We present the design of a wide-band low-noise amplifier (LNA) implemented in 0.35μm SiGe BiCMOS technology for cable and terrestrial tuner applications. The LNA utilizes current injection to achieve high linearity. Without using inductors, the LNA achieves 0.1～1GHz wide bandwidth and 18.8dB gain with less than 1.4dB of gain variation. The noise figure of the wideband LNA is 5dB, and its 1dB compression point is -2dBm and IIP3 is 8dBm. The LNA dissipates 120mW of power with a 5V supply.

Key words: BiCMOS; wide band; noise figure; linearity; low-noise amplifier; SiGe
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1 Introduction

In modern integrated RF receivers, the low noise amplifier (LNA) is one of the most critical building blocks since its NF, gain, and linearity contribute significantly to the overall system performance. Wide-band LNAs are used in terrestrial, cable, and other applications in which the ratio between bandwidth and center frequency can be larger than two. For narrow-band LNAs, low noise figure, high gain, and impedance matching can be achieved at relatively low power consumption by exploiting the quality factor of coil-based matching networks[1]. However, this is not practical for wide-band receivers as in cable digital video reception (100～1000MHz bandwidth in China), satellite reception (950～2150MHz), and terrestrial reception (450～850MHz) due to the complexity of the required wide-band matching networks. For wide band reception, the wide-band nature of transistors and resistors is typically used. As the demand for increased bandwidth grows, designing wide-band LNAs becomes more difficult.

This paper presents the design of a wide-band LNA implemented in 0.35μm SiGe BiCMOS technology for digital video broadcasting via cable (DVB-C) and terrestrial (DVB-T) tuner applications. The LNA achieves an 18.8dB gain, 5dB noise figure, and -2dBm P_{1dB} over a 0.1～1GHz bandwidth. The LNA dissipates less than 120mW of power with a 5V power supply.

2 Design of wide-band LNA circuit

Traditional wide-band LNAs often use a single-end cascode architecture because of its high gain at high-frequency and superior reverse isolation. However, cascode LNAs suffer from limited linearity due to the stacking of two transistors, which reduces the available output swing. On the other hand, a differential architecture relaxes the requirement for a large output swing, which improves the linearity[2]. Therefore, a differential architecture is chosen in DVB-C and DVB-T tuner systems that requires high linearity. Figure 1 shows a simplified circuit schematic of the wide-band LNA (biasing not shown). In our design, two-stage amplifiers are used.

2.1 First stage amplifier

Low noise figure, high linearity, gain, and input matching are achieved in the first stage of the wide-band LNA. A differential cascode architecture

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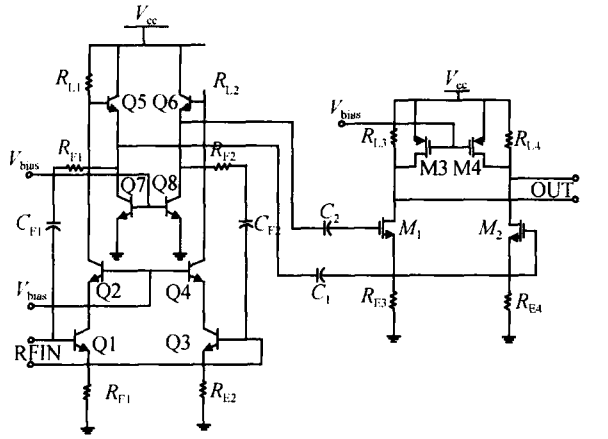

Fig. 1　Simplified circuit diagram of the wideband LNA

is chosen in the first stage for its excellent gain at high frequency and superior reverse isolation. When analyzing the small signal model of the circuit ,a single input is used instead of differential inputs.

The transistors are biased close to the peak f_T to achieve the minimum noise figure. Actually ,the current we chose is a little lower than the peak current because of manufacturing tolerance.

In our design , emitter degeneration resistors R_E are required to meet the high linearity requirements. Using the small signal model , the third-order intercept voltage can be approximately determined by[3]

$$\begin{aligned} V_{IP3} &= 2\sqrt{\frac{k_1}{3k_3}} \\ &= 2\sqrt{\frac{1}{3}} \times \frac{1}{|R_E + r_e|} \times \sqrt{\frac{6I_C^2 |R_E + r_e|^5}{r_e |2R_E - r_e|}} \\ &= 2\sqrt{2}v_T \frac{|R_E + r_e|^2}{\sqrt{r_e^3 |2R_E - r_e|}} \\ &= 2\sqrt{2}v_T \left(\frac{R_E + r_e}{r_e}\right)^{\frac{3}{2}} \end{aligned} \tag{1}$$

where v_T is the thermal voltage ,and r_e and R_E are the emitter resistances of the transistor and the emitter degeneration resistor ,respectively. Thus ,the size of the emitter degeneration resistor R_E can be obtained from the IP3 requirement by the equation

$$R_{E1} = R_{E2} = R_E = r_e \left(\frac{V_{IP3}}{2v_T}\right)^{\frac{2}{3}} \tag{2}$$

The output resistances R_{L1} and R_{L2} are used to obtain the first stage gain. Unlike the traditional LNA ,the output resistances here must allow the maximum signal that satisfies the high linearity requirement to pass the first stage without distortion.

For optimum NF ,the LNA has to be matched to the optimum source impedance. Shana 'a *et al*. derived the relationship between optimum source impedance and the transistor size as[4]

$$\begin{aligned} R_{S\text{-}opt}(M) &= \frac{1}{MN} \times \left\{ \frac{f_T}{f}\left(\frac{n^2 V_T}{2J_C} + (r_e + r_b)_u\right) \times \right. \\ &\left. \left(\frac{\sqrt{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{4\beta_{DC} f^2}}}{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right)} \right) \right\} \\ &= \frac{1}{MN} A_{(J_C, f)} \end{aligned} \tag{3}$$

where MN represents the device 's size ,and $A_{(J_C, f)}$ is a constant for fixed current density J_C and frequency f. Unfortunately ,it is difficult to match the optimum source impedance to the cable input impedance for wide band. Thus ,a shunt feedback has to be used , and then the transistors will have a much smaller bearing on the noise figure than in a tuned LNA ,while matching the power.

The simple shunt feedback circuit and its small signal model are shown in Fig. 2. Resistor R_f forms the feedback ,and capacitor C_f is added to allow for independent biasing of the base and collector[3]. Ignoring the Miller effect and assuming that C_f is a short circuit ($1/\omega C_f \ll R_f$) and r_b is low compared to r_{be} ,the input impedance can be given by

$$\begin{aligned} Z_{in} &= \frac{Z_{be}(R_f + R_l)}{R_f + R_l + Z_{be}(1 + g_m R_l)} \\ &\approx R_f \parallel Z_{be} \parallel \frac{R_f + R_l}{g_m R_l} \approx \frac{R_f + R_l}{g_m R_l} \end{aligned} \tag{4}$$

As a result ,compared to the open-loop amplifier input impedance Z_{be} ,the input impedance for the shunt feedback amplifier has less variation over wide band frequency and process. Then wide band match is achieved.

In our design ,since the voltage gain is greatly affected by the feedback[3] ,a buffer between the first stage and the second stage is added. The buffer can also provide some inductance to the input , which tends to make the match better and provide matching between the two stages. As shown in Fig. 1 , R_{F1} and R_{F2} are shunt-feedback resistors ,and transistors Q5～Q8 make up the buffer. The buffer is assumed to be lossless ,and the input impedance

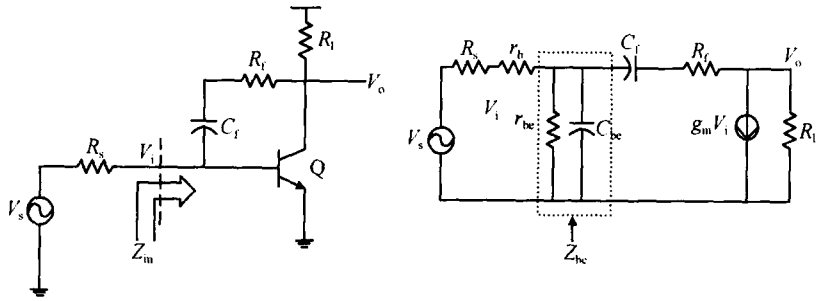

Fig. 2 Simple shunt feedback circuit and small signal model

becomes

$$Z_{in} = Z_{be}\left(1 + \frac{Z_{be}}{R_F} + \frac{g_m R_L Z_{be}}{R_F}\right)^{-1} = \frac{R_F}{1 + g_m R_L + \frac{R_F}{Z_{be}}} \approx \frac{R_F}{g_m R_L} = \frac{R_F}{G_O} \quad (5)$$

Since input impedance of the LNA can be estimated by the feedback resistance R_F divided by the open loop gain[5,6], the size of the feedback resistance can be determined:

$$Z_{in} \approx \frac{R_F}{G_O} = \frac{R_F}{\frac{R_L}{R_E + r_e}} \Rightarrow$$

$$R_{F1} = R_{F2} = R_F = \frac{Z_{in} R_L}{R_E + r_e} \quad (6)$$

With the addition of a buffer, the voltage gain is no longer affected by the feedback, and the gain of the first stage can be estimated by the open-loop gain minus the loss in the buffer:

$$G_1 \approx -\frac{R_L}{R_E + r_e} G_{BO} \quad (7)$$

Here, G_{BO} is the voltage gain of buffer.

The feedback also results in the reduction of the role transistors play in determining the gain, and it therefore improves linearity[3], but the presence of feedback resistors R_{F1}, R_{F2} may degrade the noise.

2.2 Second stage amplifier

If the second stage of the common emitter amplifier were not used, the two transistors of the cascode and the emitter resistors in first stage would consume a large voltage, which would limit the headroom. Then it would be impossible to achieve high linearity. This is the reason why it is difficult to achieve high linearity and high gain simultaneously with traditional LNAs. Therefore the common source amplifier is added after first stage, which can broaden the headroom of the cascode and provide some gain.

Transistors M1～M4 and some resistors compose the second stage. Then the total voltage gain can be approximated as

$$G_{tot} = G_1 G_2 = \frac{R_L R_L'}{(R_E + r_e)(R_E' + r_e')} G_{BO} \quad (8)$$

where R_L and R_L' represent the load resistors of the two stages, respectively, R_E and R_E' represent the emitter degeneration resistors of the two stages, r_e and r_e' are the emitter resistors of the transistors in the two stages, and G_{BO} is the voltage gain of the buffer.

In the design, the method of current injection is introduced to improve the linearity in the second stage. In high frequency LNAs, the input third-order intercept point (IIP3) is relative to the collector current[4,7]. When a signal passes the first stage, it becomes large. Hence, a large collector current is needed to satisfy the high linearity. However, it is difficult to size the load resistor because of the large current. High linearity can be achieved, but at the expense of gain. The current injection technique is good at solving this problem, but this technique is rarely used in the design of low noise amplifiers because much noise results from adding a current source. However, this method can be used in the second stage. The noise factor of an N-stages connected system is[8]

$$F = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_N - 1}{A_1 A_2 \cdots A_{N-1}} \quad (9)$$

where F_i and A_i are the noise factor and gain of each stage, respectively. From Eq. (9), it can be seen that the noise of the current source in the second stage will contribute almost nothing to the total system. Thus, in our design, two current sources are added to the load in the second stage, which improves the headroom problem without

adding much noise to the system. In addition, high linearity and high gain can be obtained simultaneously. As shown in Fig. 1, pMOS transistors M3 and M4 make up the current sources, which afford a part of the current from transistors M1 and M2. The simulation result indicates that the NF of the LNA with current injection is 0.3dB, which is larger than that for the same architecture LNA without current injection. But the IIP3 is increased by 3.8dB.

3 Measured and simulated results

The wide band LNA is implemented using standard 0.35μm SiGe BiCMOS technology. All of the simulated results come from a Cadence Spectre simulator.

3.1 Direct current analysis

The measured result shows that the DC power consumption P_{dc} is 120mW, which is below the design goal of 200mW, with a 5V voltage supply. This power consumption is suitable for DVB-C and DVB-T tuner systems, in which power consumption is not a concerned parameter.

3.2 Gain analysis

In the simulation and testing, the frequency of the input signals was from 100MHz to 1GHz. The voltage gain (G_{tot}) here is defined as the output voltage divided by the input voltage. Measured and simulated results of the gain are shown in Fig. 3. The typical voltage gain of the wide band LNA is 18.8dB with 1.4dB gain flatness from 100MHz to 1GHz. The gain reaches its maximum of 20.2dB at 300MHz, and its minimum of 17.5dB at 1GHz.

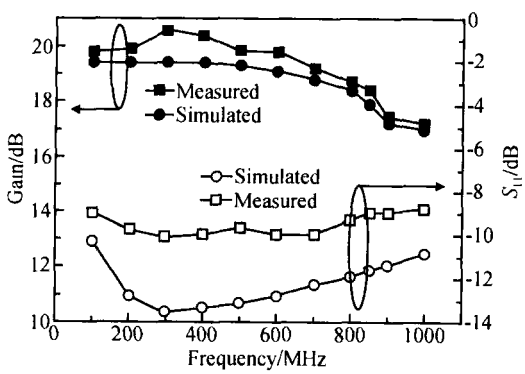

Fig. 3　Measured and simulated results of LNA gain and S_{11}

3.3 S-parameter analysis

S-parameters are tested to verify the input matching. Figure 3 shows the measured and simulated results of S_{11}. As shown in Fig. 3, S_{11} is lower than -9dB throughout the whole frequency band, showing a good broad-band input match. But the measured result is a little worse than the simulation due to the parasitic effect on the testing board.

3.4 Noise figure analysis

In Fig. 4, the measured result shows that in the whole frequency band, the typical noise figure (NF) is less than 5dB, which meets the design goal. It can be seen from Fig. 4 that the measured NF is about 1dB more than the simulation due to the noise coming from the balun in the testing.

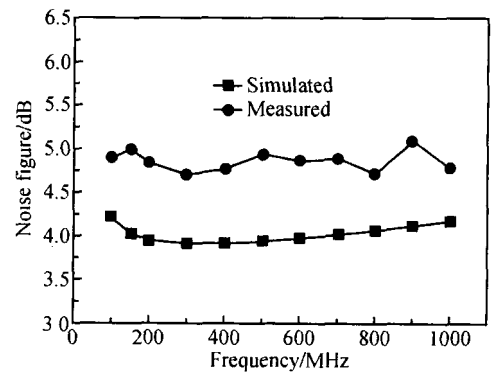

Fig. 4　Measured and simulated LNA noise figures

3.5 Linearity analysis

Power measurement is performed at 900MHz to evaluate the high frequency behavior. As shown in Fig. 5, the measured input power -1dB compression point is -2dBm. This is a very high linearity, while its gain is almost 19dB.

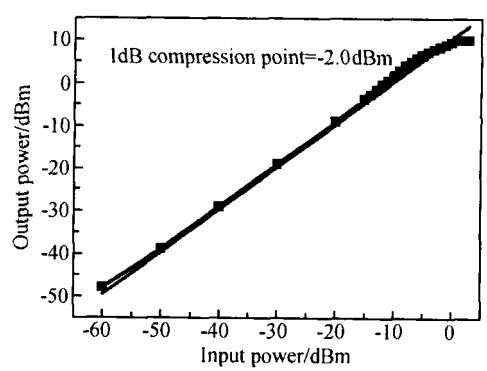

Fig. 5　Measured LNA P1dB

4 Discussion

The circuit performances presented in this paper are summarized and compared with other academic works and commercial products in Table 1.

Table 1 Performance comparison of academic and commercial wide-band LNA

Parameter	This work		Academic work		Commercial work
	Design goal	SiGe LNA	LNA in Ref. [9]	LNA in Ref. [10]	LNA in Ref. [11]
Gain/ dB	17	18.8	18	13.7	13.4
BW/ MHz	100～1000	100～1000	50～870	2～1600	100～1300
NF/ dB	5	5	5	2.5	3.8
S_{11}/ dB	- 10	- 9	- 11	- 8	- 18
P_{1dB}/ dBm	0	- 2	- 10	- 9	- 22
I_{CC}/ mA ,V_{CC}/ V	40 ,5	24 ,5	NA ,3.3	14 ,2.5	8 ,5
Chip/ mm^2		0.9 ×0.5	NA	0.3 ×0.25	NA
Year		2005	2005	2004	2001

Compared with other works, the wide-band LNA in this paper has an excellent combination of gain, linearity, noise figure, power consumption and impedance matching. The circuit in Ref. [9] has superior gain, but its linearity would not fit our design goals. The LNAs in Refs. [10] and [11] have good noise figure and lower power dissipation, but poor gain and linearity. The NF of the LNA in this paper is worse than that in Ref. [10] due to the differential architecture, the presence of feedback resistors, and the use of current injection technology. But a 5dB noise figure in the whole frequency band is suitable for DVB tuner systems.

5 Conclusion

In this paper, a SiGe wide band LNA with excellent gain, linearity, noise, impedance matching, and bandwidth for DVB-C and DVB-T tuner applications is presented. The wideband LNA achieves an 18.8dB gain, - 2dBm P_{1dB}, 8dBm input IP3, and 5dB noise figure, which meet the requirements for DVB-C and DVB-T tuner applications. The proposed current injection demonstrates good performance for high linearity LNA design. The LNA occupies a 0.9mm ×0.5mm die area as shown in Fig. 6 and consumes 120mW of power with a 5V supply.

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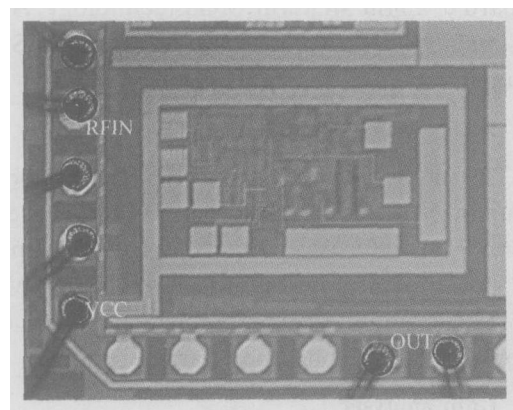

Fig. 6 Die photo of SiGe LNA prototype

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一种用于地面和有线接收机的宽带低噪声放大器*

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摘要: 提出并设计了一种用于数字电视接收调谐芯片的宽带低噪声放大器. 该设计采用 0.35μm SiGe BiCMOS 工艺, 器件的主要性能为: 增益等于 18.8dB, 增益平坦度小于 1.4dB, 噪声系数小于 5dB, 1dB 压缩点为 -2dBm, 输入三阶交调为 8dBm. 在 5V 供电的情况下, 直流功耗为 120mW.

关键词: BiCMOS; 宽带; 噪声系数; 线性度; 低噪声放大器; SiGe
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